Description of LPDDR3 Bus Violation Parameters

- Based on JESD209-3B
- All values in nCK (number of clock cycles), unless marked with [ns]
- Example values based on 8GB, 1600/1.25nS, and tWL=6, tRL=12
- Temperature derating add 1.875 nS when MR4 [2:0] = 110 to tRRD, tRCD, tRC, tRAS, tRP
- Assume: all ranks identical devices and latencies.
- Assume: fixed burst size.
- Note ODTSEL is not applicable to LPDDR3 and is not implemented.

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for LPDDR3 mode	Ex.	Qty
1	MRR to non-NOP < tMRR_cc	SR	tMRR_cc 4 b ENABLE 1 b	tMRR_cc = tMRR	4	4
2	MRW to non-NOP < tMRW_cc	SR	tMRW_cc 6 b ENABLE 1 b	tMRW_cc = tMRW	10	4
3	ACT to Rd or Wr < tRCD_cc	SB	tRCD_cc 6 b ENABLE 1 b	tRCD_cc = tRCD[ns]/tCK[ns]	14	32
4	PREA to non-NOP < tRPab_cc PREA to REF, ZQCL, ZQCS, ZQRESET, ZQINIT, or MRW < tRPab_cc	SR SR	tRPab_cc 6 b ENABLE 1 b	tRPab_cc = tRPab[ns]/tCK[ns]	22	32
5	PRE to ACT < tRPpb_cc PRE to REF, ZQCL, ZQCS, ZQRESET, ZQINIT, or MRW < tRPpb_cc	SB SR	tRPpb_cc 6 b ENABLE 1 b	tRPpb_cc = tRPpb[ns]/tCK[ns]	19	32
6	Rd to PRE < tRTP_cc Rd to PREA < tRTP_cc	SB SR	tRTP_cc 6 b ENABLE 1 b	tRTP_cc = BL/2 + max(4, tRTP[ns]/tCK[ns]) - 4	6	32
7	Wr to Wr < tCCD_cc	SR	tCCD_cc 4 b ENABLE 1 b	tCCD_cc=tCCD	4	4
8	REFab to non-NOP <tRFCab_cc	SR	tRFCab_cc 10b ENABLE 1 b	tRFCab_cc= tRFCab[ns]/tck[ns]	168	4
9	REFpb to non-NOP < tRFCpb_cc	SR	tRFCpb_cc 10b ENABLE 1 b	tRFCpb_cc= tRFCpb[ns]/tck[ns]	72	4
10	SRX followed by non-NOP within tXSR_cc	SR	tXSR_cc 10b ENABLE 1 b	tXSR_cc=tXSR[ns]/tck[ns]	176	4

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Chk #	Violation Hardware Specification	App.	Parameters	PM Equation for LPDDR3 mode	Ex.	Qty
11	Self Refresh time less than tCKESR_cc	SR	tCKESR_cc 4 b ENABLE 1 b	tCKESR_cc= tCKESR[ns]/tck[ns]	12	4
12	ACT to ACT or REFpb < tRRD different banks	SR	tRRD_cc 4 b ENABLE 1 b	tRRD_cc=tRRD[ns]/tck[ns]	8	4
13	ACT to PRE < tRASmin_cc ACT to PREA < tRASmin_cc	SB SR	tRASmin_cc 6 b ENABLE 1 b	tRASmin_cc = RU(tRASmin[ns]/tCK[ns])	34	32
14	ACT to PRE > tRASmax_cc ACT to AP > tRASmax_cc ACT to PREA > tRASmax_cc	SB SB SR	tRASmax_cc 17b ENABLE 1 b	tRASmax_cc = RU(tRASmax[ns]/tCK[ns])	56000	32
15	Read to Write < tSR_RTW_cc Fixed burst size 8	SR	tSR_RTW_cc 5 b ENABLE 1 b	tSR_RTW_cc = RL - WL + BL/2 +1 + RU(tDQSCKmax[ns]/tCK[ns])	19	4
16	Write to PRE < tWTP_cc Write to PREA < tWTP_cc Fixed burst size 8	SB SR	tWTP_cc 6 b ENABLE 1 b	tWTP_cc = WL + BL/2 + 1 + RU(tWR[ns]/tCK[ns])	22	32
17	Write to Read < tSR_WTR_cc Fixed burst size 8	SR	tSR_WTR_cc 6 b ENABLE 1 b	tSR_WTR_cc = WL + BL/2 + 1 + RU(tWTR[ns]/tCK[ns])	17	4
18	Read or Write to an Inactive Bank	SB	ENABLE 1 b			32
19	REFab to an Active Bank	SB	ENABLE 1 b			32
20	Activate to an Active Bank	SB	ENABLE 1 b			32
21	Read to Read < tSR_RTR_cc	SR	tSR_RTR_cc 4 b ENABLE 1 b	tSR_RTR_cc=tCCD	4	4
22	Read to Read < tDR_RTR_cc Fixed burst size 8	DR	tDR_RTR_cc 4 b ENABLE 1 b	tDR_RTR_cc= BL/2 +1 + RU(tDQSCKmax[ns]/tCK[ns]) - RU(tDQSCKmin[ns]/tCK[ns])	5	4
23	Read to Write < tDR_RTW_cc Fixed burst size 8	DR	tDR_RTW_cc 6 b ENABLE 1 b	tDR_RTW_cc = RL + RU(tDQSCKmax[ns]/tCK[ns]) + BL/2 +1 -WL - RU(tDQSSmin[ns]/tCK[ns])	20	4

Chk #	Violation Hardware Specification	App.	Parameters	PM Equation for LPDDR3 mode	Ex.	Qty
24	Write to Read < tDR_WTR_cc Fixed burst size 8	DR	tDR_WTR_cc 6 b ENABLE 1 b	tSR_WTR_cc = WL + BL/2 + 1 + RU(tDQSSmax[ns]/tCK[ns]) - RL - RU(tDQSCKmin[ns]/tCK[ns])	16	4
25	Write to Write < tDR_WTW_cc Fixed burst size 8	DR	tDR_WTW_cc 4 b ENABLE 1 b	tDR_WTW_cc= BL/2 +1 + RU(tDQSSmax[ns]/tCK[ns]) - RU(tDQSSmin[ns]/tCK[ns])	5	4
26	Average REFab Interval > tREFI_cc	SR	tREFI_cc 14b ENABLE 1 b	tREFI_cc= RU (tREFI [ns]/tCK[ns])	3120	4
27	MRW-ZQCS to non-NOP or ODT < tZQCS_cc	SR	tZQCS_cc 8 b ODTEN 1 b ENABLE 1 b	tZQCS_cc = RU(tZQCS[ns]/tCK[ns])	72	4
28	MRW-ZQCL to non-NOP or ODT < tZQCL_cc	SR	tZQCL_cc 10b ODTEN 1 b ENABLE 1 b	tZQCL_cc = RU(tZQCL[ns]/tCK[ns])	288	4
29	MRW-ZQINIT to non-NOP or ODT < tZQINIT_cc	SR	tZQINIT_cc 11b ODTEN 1 b ENABLE 1 b	tZQINIT_cc = RU(tZQINIT[ns]/tCK[ns])	800	4
30	MRW-ZQRESET to non-NOP or ODT < tZQRESET_cc	SR	tZQRESET_cc 8 b ODTEN 1 b ENABLE 1 b	tZQRESET_cc = RU(tZQRESET[ns]/tCK[ns])	40	4
31	5 ACT in less than tFAW_cc	SR	tFAW_cc 6b ENABLE 1 b	tFAW_cc= tFAW[ns]/tCK[ns]	40	4
32	Read to CKE low < tREAD_cc	SR	tREAD_cc 6b ENABLE 1 b	tREAD_cc = RL + RU(tDQSCKmax[ns]/tCK[ns]) + BL/2 +1	21	
33	Write to CKE low < tWRITE_cc	SR	tWRITE_cc 6b ENABLE 1 b	tWRITE_cc = WL + 1 + BL/2 +RU(tWR[ns]/tCK[ns])	23	
34	CKE assert time < tCKEmin_cc	CKE	tCKEmin_cc 4b ENABLE 1 b	tCKEmin_cc = tCKEmin[ns]/tCK[ns]	6	4
35	Enter PD, SREF,DPD followed by non-NOP < tCPDED_cc (Two NOP commands are required after CKE goes low)	SR	tCPDED_cc 4b only valid values =1,2 or 3 ENABLE 1 b	tCPDED_cc = tCPDED	2	4
36	Deep Power Down time < tPDmin_cc	SR	tDPDmin_cc 20b ENABLE 1 b	tDPDmin_cc = tDPDmin[ns]/tCK[ns]	400K	4

Chk #	Violation Hardware Specification	App.	Parameters	PM Equation for LPDDR3 mode	Ex.	Qty
37	PDX followed by non-NOP within tXPmin_cc	SR	tXPmin_cc 4b ENABLE 1b	tXRmin_cc = tXPmin[nS]/tck[ns]	6	4

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