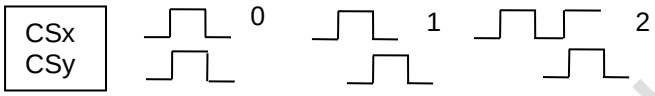
Description of DDR3 Bus Violation Parameters for the FS2800 DDR Detective®

This setup starts with a checklist of all JEDEC based DDR3 SDRAM protocol parameters that are available to be checked by the FS2800 DDR Detective. Once a particular protocol attribute is selected then a detail box is shown on the right. The detail box shows the JEDEC parameters that are specific for that violation and the corresponding default values of those parameters. The default values can be modified and the range accepted is listed in parentheses.

Refer to JEDEC DDR3 SDRAM Standard JESD79-3E for definitions and details on these specs.

Note 1. Applicability of check: Any = any occurrence, SR = Same Rank, SB = Same Bank DR = Same DIMM Different Rank DD = Different DIMM

Note 2. The minimum value for any parameter is 2 (to prevent malfunction)
Exception: tCSGAP uses 0 latency value to disable latency check. Otherwise minimum value is 1



Exception: tCPDED is a special case requiring a minimum value of 1.

Note 3. **ODTSEL** is a control register bit that affects the ODT portion of the check.
For cases where Rtt are turned off via MRS, set **ODTSEL** = 0 and the protocol checkers will test for a static level rather than a low level on ODT.

Note 7. Large counters (56,000 tCK range) have reduced precision and extra latency as follows:
Can trigger at any 1 of the following values: threshold -2, threshold -1, threshold, threshold +1
PM could set accordingly to avoid false violation detects by using min value plus 2 (in a minimum test), or max value minus 1 (in a maximum test)
The violation will also be reported late as follows: PV and PC will assert 4 tCKs late.

Chk #	Violation test	App	Corresponding JEDEC parameter
1	MRS to MRS < tMRDmin MRS to other command or ODT (Note 3.) or CKE low <tMOD	SR SR	tMRD = tMRDmin tMOD = tMODmin
2	ACT to Rd or Wr < tRCD	SB	tRCD = tRCDmin[ns]/tCK[ns] - AL
3	PRE to ACT <tRP PREA to ACT <tRP PRE or PREA to REF <tRP PRE or PREA to ZQCL <tRP PRE or PREA to ZQCS <tRP PRE or PREA to MRS <tRP PRE or PREA to SRE <tRP	SB SR SR SR SR SR SR	tRP = tRPmin[ns]/tCK[ns]
4	Rd to PRE <tRTP Rd to PREA <tRTP	SB SR	tRTP = tRTPmin + AL
5	Wr to Wr < tCCD	SR	tCCD = tCCDmin
6	REF to non-NOP/DES <tRFC non-NOP/DES includes CKE low	SR	tRFC = tRFCmin[ns]/tck[ns]
7	SRX followed by non-NOP/Des within tXS non-NOP/DES includes CKE low	SR	tXS = tXSmin
8	Self Refresh time less than tCKESR	SR	tCKESR = tCKESRmin
9	SRX followed by Read or ODT (Note 3.) or CKE low (other than SRE following a REF) within tXSDLL	SR	tXSDLL = tXSDLLmin
10	ACT to ACT <tRRD different bank	SR	tRRD = tRRDmin

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Chk #	Violation	App	Corresponding JEDEC parameter
11	Any CS# asserted for >1 cycle or any CS# to any CS# < tCSGAP See note 2	Any	tCSGAP = 0 for no gap "1N" tCSGAP = 2 for gap =1 "2N" tCSGAP = 3 for gap =2 "3N"
12	ACT to PRE < tRASmin	SB	tRASmin = roundup (tRASmin[ns]/tCK[ns])
13	ACT to PRE > tRASmax_cc ACT to AP > tRASmax_cc ACT to PREA > tRASmax_cc (must see the Activate) Extra latency See Note 7	SB SB SR	tRASmax_cc = roundup(9*tREFI [ns]/tCK[ns] Threshold +1/-2 See Note 7
14	Read to Write < tSR_RTW There are 2 turnaround cycles	SR	tSR_RTW_cc = RL - WL + tCCD +2 (Read: Fixed BL8 or OTF BL8) not supported: tSR_RTW_cc = RL - WL + tCCD/2 +2 (Read: OTF BC4)
15	Write to PRE < tWTP Write to PREA < tWTP Reference: JEDEC Pg 72, Fig. 50, 51	SB SR	tWTP = WL + roundup(tWR[ns]/tCK[ns]) +4 (BL = Fixed 8 or OTF8, 4) tWTP = WL + roundup(tWR[ns]/tCK[ns]) +2 (BL = Fixed BC4)
16	Write to Read < tSR_WTR Reference: JEDEC Pg 72-75, Figs 49, 54, 55, 56 (tSR_WTR is not a JEDEC name	SR	tSR_WTR = WL + tWTRmin + 4 (BL = Fixed 8 or OTF) tSR_WTR = WL + tWTRmin + 2 (BL = Fixed 4)
17	Read or Write to an Inactive Bank (Must see RESET# or PRE/PREA to know banks are inactive.)	SB	
	Refresh to an Active Bank (Must see RESET# or PRE/PREA to know banks are inactive.)	SB	
	Activate to an Active bank (Must see 1st Activate to know bank is active.)	SB	
	MRS with an Active Bank (Must see Activate to know bank is active.)	SR	
	Self Refresh entry with an Active Bank	SR	
	ZQCS or ZQCL with an Active bank	SR	

Note 2. The minimum value for any parameter is 2 (to prevent malfunction)
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Chk #	Violation	App	Corresponding JEDEC parameter
18	Spare		
19	Read to Read < tSR_RTR	SR	tSR_RTR = tCCDmin
20	Read to Read < tDR_RTR	DR	tDR_RTR_cc=4 +? (fixed BL8) =2 +? (fixed BC4)
21	Read to Read < tDD_RTR	DD	tDD_RTR_cc=4 +? (fixed BL8) =2 +? (fixed BC4)
22	Read to Write < tDR_RTW	DR	tDR_RTW_cc = RL - WL + 4 +? (fixed BL8) = RL - WL + 2 +? (fixed BC4)
23	Read to Write < tDD_RTW	DD	tDR_RTW_cc = RL - WL + 4 +? (fixed BL8) = RL - WL + 2 +? (fixed BC4)
24	Write to Read < tDR_WTR	DR	tSR_WTR_cc = WL - RL + 4 +? (fixed BL8) = WL - RL + 2 +? (fixed BC4)
25	Write to Read < tDD_WTR	DD	tSR_WTR_cc = WL - RL + 4 +? (fixed BL8) = WL - RL + 2 +? (fixed BC4)
26	Write to Write < tDR_WTW	DR	tDR_WTW_cc =4 +? (fixed BL8) =2 +? (fixed BC4)
27	Write to Write < tDD_WTW	DD	tDD_WTW_cc =4 +? (fixed BL8) =2 +? (fixed BC4)
28	Refresh to Refresh > tREFIMAX Average Refresh Interval over the last 128 refreshes > tREFI	SR SR	tREFIMAX = roundup (9*tREFI [ns]/tCK[ns]) tREFI = roundup (tREFI [ns]/tCK[ns])
29	ZQCS to non-NOP/DES, or ODT (Note 3.) < tZQCS ZQCL to non-NOP/DES, or ODT (Note 3.) < tZQoper non-NOP/DES includes CKE low	SR SR	tZQCS = tZQCS tZQoper = tZQoper
30	Write w/AP to ACT < tDAL Write w/AP to REF < tDAL Write w/AP to ZQCS < tDAL Write w/AP to ZQCL < tDAL Write w/AP to MRS < tDAL Write w/AP to SRE < tDAL (Write w/AP to PDE < tDAL)	SB SR SR SR SR SR	tDAL = CWL + WR + roundup(tRPmin[ns]/tCK[ns])
31	5 ACT in less than tFAW	SR	tFAW = tFAW[ns]/tCH[ns]

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Chk #	Violation	App	Corresponding JEDEC parameter
32	Read to CKE low or MRS < tREAD Write to CKE low or MRS < tWRITE	SR SR	tREAD = CL + AL +4 (BL = Fixed8 or OTF) tREAD = CL + AL +2 (BL = Fixed4) tWRITE = CWL + AL + roundup(tWR[ns]/tCK[ns]) +4 (BL = Fixed8 or OTF) tWRITE = CWL + AL + roundup(tWR[ns]/tCK[ns]) +2 (BL = Fixed4)
33	MR0 DLL reset followed by Read or ODT (Note 3.) or CKE low < tDLLK.	SR	tDLLK = tDLLK
34	ODT hi to low time <ODTH4_cc or Write with ODT hi to low time < ODTH4_cc (When BL=Fixed4 or BL=OTF and burst chopped) Write with ODT hi to low time < ODTH8_cc (When BL = Fixed8 or BL = OTF & not chopped) See Note 8.	Any Any	ODTH4 = ODTH4 ODTH8 = ODTH8
35	CKE assert time < tCKE	SR	tCKEmin = tCKEmin
36	PDE followed by non-NOP/DES < tCPDED	SR	tCPDED = tCPDED
37	Power Down min time < tPDmin	SR	tPDmin = tPDmin = tCKEmin
38	Power Down max time < tPDmax Extra latency See Note 7	SR	tPDmax = tPDmax = roundup (9*tREFI [ns]/tCK[ns]) Threshold +1/-2 See Note 7
39	PDX fast exit: PDX followed by any command within tXP	SR	tXP = tXPmin
40	PDX slow exit: Exit from Precharged Power Down followed by Read or ODT (see Note 3.) within tXSDLL_cc. Valid only when MR0 A12 is 0.	SR	tXPDLL = tXPDLL

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