Description of the LPDDR4 Bus Violation Parameters

- Based on the JEDEC LPDDR4 Specification
- All Values in nCK (number of clock cycles), unless marked with [ns]
- Assumes all ranks identical devices and latencies

	Violation Hardware Specification	App	PV Equation for LPDDR4 mode	Spec. reference Updated for Published B spec
1	REFpb to REFab/ACT(same bank)/REFpb(same bank) < tRFCpb_cc	SR SB	tRFCpb_min = RU(tRFCab/tCK)	Table 44, section 4.19
2	REFab to REFab/ACT/REFpb < tRFCab_cc	SR	tRFCab_min = RU(tRFCab/tCK)	Table 44, section 4.19
3	REFpb to ACT < tRRD_cc REF to REF < tRRD_cc	SR	tRRD_min = max(RU(10ns/tCK), 4nCK)	Table 41
4	ACT to ACT < tRRD_ACT_cc	SR DB	tRRD_ACT_min = max(RU(10ns/tCK), 4nCK)	Table 17,34 Sec. 4.1 Figure 6
5	ACT to RD or WR < tRCD_cc	SB	tRCD_min = max(RU(tRCD[ns]/tCK[ns]), 4nCK	Table 17, section 4.1 figure 6
6	ACT to ACT < tRC_pb_cc With PRE per bank between ACT's	SR	tRC_pb_min = tRASmin + tRPpb tRASmin = max(RU(42ns/tCK), 3nCK) tRPbp = max(RU(18ns/tCK), 4nCK)	Table 17, section 4.18 Figure 6
7	ACT to ACT < tRC_ab_cc With PREA between ACT's	SR	tRC_ab_min = tRASmin + tRPab tRAS = max(RU(42ns/tCK), 3nCK) tRPab = max(RU(21ns/tCK), 4nCK)	Table 17, section 4.18
8	ACT to PRE/PREA < tRAS_Min_cc	SB SR	tRAS_Min = max(RU(42ns/tCK), 3nCK)	Table 17,

				section 4.18
9	ACT to PRE/PREA > tRAS_Max_cc	SB SR	tRAS_Max = Min RU((9 * tREFI)/tCK) (Refresh Rate = 70.2 us)	Table 17, section 4.15, Table 32
10	More than 4 ACT's/REFpb < tFAW_CC	SR	tFAW_min= RU(40ns/tCK)	Table 17, figure 7 and section 4.2
11	PRE to ACT/REFpb/REFab < tRPpb_cc	SB SR	tRPpb_min = max(RU(18ns/tCK),4nCK)	Table 17
12	PREA to ACT/REFpb/REFab < tRPab_cc	SR	tRPab_min = max(RU(21ns/tCK), 4nCK	Table 17
13	RD/RDA to RD/RDA < tCCD_RD_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tCCD_RD_min = BL/2	Table 26-1, Figure 31
14	RD/RDA to WR, WRA, MASK-WR, MASK-WRA < tSR_RWR_cc Subtracts 8 @ BL16 OTF[2]	SR	tSR_RTW_min = RL+RU(tDQSCK(max)/tCK)+BL/2+ RD(tRPST)-WL+tWPRE1	Table 32, section 4.15.1
15	RD to PRE or PREA < tRTP_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tRTP_min = tRTP = max(RU(7.5ns/tCK), 8nCK) +((BL/16-1) * 8)	Table 32, section 4.15.1
16	RDA to RD, RDA < tCCD_RDA_cc Subtracts 8 @ BL16 OTF[2]	SR DB	tCCD_RDA_min = BL/2	Section 4.14, section 4.15.1, Table 17
17	RDA to WR, WRA, MASK-WR, MASK WRA < t CCD_RWODT_cc Subtracts 8 @ BL16 OTF[2]	SR	t CCD_RWODT_min = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) – ODTLon – RD(tODTon,min/tCK) + 1 Enabled when using ODT	Table 39, section 4.17.4, Table 84, Table 85
18	RDA to ACT < tRRAP_cc	SB	tRRAP_min = nRTP + tRPpb + ((BL/16-1) * 8)	Table 38,

	Subtracts 8 @ BL16 OTF[2]		tRPpb = max(RU(18ns/tCK), 4nCK)	section 4.17.4, Table 28
19	RD/RD FIFO/RD DQ CAL to MRW < tRD_MRWcc	SR	RD_MRW_min = RL + BL/2+RU(tDQSCKmax/tCK)+RD(tRPST)+max(RU(7.5 ns/tCK),8nCK) Set BL for the RD cmd.	Table 50, section 4.25
20	RDA to MRW < tRDA_MRWcc Subtracts 8 @ BL16 OTF[2]	SR	RDA_MRW_min = RL+BL/2+RU(tDQSCKmax/tCK) + RD(tRPST) +max(RU(7.5ns/tCK),8nCK)+nRTP-8	Table 50, section 4.25
21	WRA to RD, RDA < tWTR_WRRD_cc Subtracts 8 @ BL16 OTF[2]	SR	tWTR_WRRD_min = WL + BL/2 +RU(tWTR/tCK) + 1 tWTR = max(10ns, 8nCK)	Table 38, section 4.18.1, Table 17
22	WR to PRE or PREA < tWR_WRPRE_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tWR_WRPRE_min = WL + BL/2 + (tWR/tCK) + 1 tWR= max(18ns, 6nCK)	Table 38, section 4.18.1, Table 17
23	WRA to PRE or PREA < tWR_WRAPRE_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tWR_WRAPRE_min = WL + BL/2 + nWR + 1	Table 38, section 4.18.1
24	WR to MASK-WR < tCCDMW_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tCCDMW_min = 4*tCCD + 8	Table 17, Table 32, section 4.15.1
25	MASK-WR, WR to MASK-WR < tCCDMW_cc Subtracts 8 @ BL16 OTF[2]	SR DB	tCCDMW_min = 4 * tCCD	Table 17, Table 32, section 4.15.1
26	MASK-WR to RD, RDA < tWTR_MWRRD_cc	SR SB	tWTR_MWRRD_min = WL + 16/2 + RU(tWTR/tCK) + 1 tWTR = max(10ns, 8nCK)	Table 32
27	MASK-WR to PRE or PREA < tWR_MWRPRE_cc	SR SB	tWR_MWRPRE_min = WL + 16/2 + RU(tWR/tCK) + 1 tWR= max(18ns, 6nCK)	Table 32, Table 17

28	MASK-WRA to MASK-WR, MASK-WRA, WR, WRA < tCCD_MWRA _cc	SR DB	tWR_MWRA_min = 16/2	Table 38
29	WRA to MASK-WRA, MASK-WR,WR, WRA < tCCD_WRA _cc Subtracts 8 @ BL16 OTF[2]	SR DB	tWR_WRA_min = BL/2	Table 38
30	MASK-WRA to ACT < tWR_MACT_cc	SR SB	tWR_MACT_min = WL + 16/2 + nWR + 1 + (tRPpb/tCK) tRPpb = max(18ns, 4nCK)	Table 38,Table 17
31	WRA to ACT < tWRAP_cc Subtracts 8 @ BL16 OTF[2]	SR SB	tWRAP_min = WL + BL/2 + nWR +1 + RU(tRPpb/tCK)	Table 38,Table 17
32	SRE to SRX< tSR_cc	SR	tSR_min = max(RU(tSR/tCK), 3nCK)	Table 17, section 4.3
33	SRX to non-NOP < tXSR_cc	SR	tXSR_min = max(RU((tRFCab + 7.5 ns)/tCK)), 2nCK)	Table 17, section 4.3, Table 44, Table 45
34	PDX to non NOP < tXP_cc	SR	tXP_min = max(RU(7.5ns/tCK), 5 nCK)	Table 17, section 4.3 4.48.1, Figure 137, Table 94
35	PDX to MRR < tMRRI_cc	SR	tMRRI_min = tXP + tMRRI tXP = max(7.5ns/tCK, 5 nCK) tMRRI = tRCD + 3nCK tRCD = max(18ns, 4nCK)	Table 48
36	PRE, PREA to PRE, PREA < tPPD_cc	SR	tPPD_min = 4 tCK	Table 17, 38
37	MRR to MRR, RD/RDA < tMRR_cc	SR	tMRR_min = tMRR tMRR= 8nCK	Table 48
38	MRR to WR/WRA/MASK-	SR	see 4B spec. pg 160 Enable this check when ODT is disabled	Table 50,

	WRA/MASK-WR < tMRR_MRRWR_cc		tMRR_MRRWRmin = RL + ROUNDUP(tDQSCK(max)/tCK) + BL/2 – WL+tWPRE+RD(tRPST)	section 4.25.1
39	MRR to WR/WRA/MASK-WR/MASK-WRA< tMRR_ODT_cc	SR	tMRR_ODT_min = RL + RU(tDQSCK(max)/tCK) + 16/2 + 3 – ODTLon-RD(tODTon(min)/tCK) see 4B spec. pg 161 Enable this check when ODT is enabled This check was changed to RL+RU(tDQSCK(max)/tCK)+BL/2-ODTLon-RD(tODTon(min)/tCK)+RD(tRPST)+1	Table 51, section 4.25.1
40	MRR to MRW < tMRR_MRRMRW_cc	SR	tMRR_MRRMRW_min = RL+RU(tDQSCK(max)/tCK)+16/2+ 3	Table 50, section 4.25.1
41	MRW to RD/RDA/ WR/WRA/MASK-WR/MASK-WRA < tMRD_cc	SR	tMRD_min = tMRD tMRD = max(RU(14ns/tCK), 10nCK)	Table 51, 50 section 4.25.1 Table 63
42	MRW to MRW < tMRW_cc	SR	tMRW_min = tMRW tMRW= max(RU(10ns/tCK), 10nCK)	Table 40, 49
43	WR/MASK-WR/WR FIFO to MRW< WR_MRW_cc	SR	WR_MRW_min = WL+1+BL/2+max(RU(7.5ns/tCK), 8nCK) Set BL for the WR Cmd.	Table 50, section 4.25.1
44	WRA/MASK-WRA to MRW < WRA_MWR_cc	SR	WRA_MWR_min = WL+1+BL/2+max(RU(7.5ns/tCK),8nCK)+nWR Set BL for the WRA Cmd.	Table 50, section 4.25.1
45	RD to MRR < tMRR_RD_cc	SR	tMRR_RD_min = BL/2	Table 50/51, section 4.25.1
46	WR, WRA, MASK-WR, MASK-WRA, MPC WR FIFO to MRR< tMRR_WR_cc	SR	tMRR_WR_min = WL + BL/2 + 1 + RU(tWTR/tCK) Set BL for the WR Cmd.	Table 50/51, section 4.25.1
47	RD or WR to inactive bank	SB	Ordering Violation	
48	REF to active bank	SB	Ordering Violation	
49	ACT to active bank	SB	Ordering Violation	

50	MPC to ZQCALLATCH < tZQCAL_CC	SR	tZQCAL_min = RU(tZQCAL/tCK) tZQCAL = 1 us	Table 76, section 4.41.1
51	SRE to CKE low < tESCKE_CC	SR	tESCKE_min = Max(RU(1.75ns/tCK), 3 tCK)	Table 46, section 4.21.4
52	CKE minimum pulse width(high and low) < tCKE_CC	SR	tCKE_min = Max(RU(7.5ns/tCK), 4nCK)	Table 94, section 4.48.1
53	Max of 16 refreshes within 2 * tREFI > t2XREF_CC	SR	t2XREF_min = RU(tREFI *2/tCK) tREFI = 3.9 us	Section 4.19 First sentence page 140
54	ZQCALRESET to valid CMD < tZQRESET_CC	SR	tZQRESET_CC = Max(RU(50ns/tCK), 3nCK)	Table 76, section 4.41.1
55	Out of order REFpb[3]	SR	Same bank cannot be refreshed until all banks have been refreshed.	
56	ZQCALLATCH to any valid cmd < tZQLAT_CC	SR	tZQLAT_CC = Max(RU(30ns/tCK), 8tCK)	Table 6, section 3.3.1, Figure 5
57	Required # of refresh cmds occur < tREFW_CC	SR	tREFW_CC = < 8192 refreshes in RU(32ms/tCK)	
58	Refresh Interval < tREFI*9_CC	SR	tREFI*9_CC = RU(3.9us * 9/tCK)	section 4.19
59	PRE to PDE < tPRE_PDE_CC	SR	tPRE_PDE_CC = tCMDCKE = Max(RU(1.75ns/tCK),3nCK)	Table 94,section 4.48.1
60	PREA to PDE < tPREA_PDE_CC	SR	tPREA_PDE_CC = tCMDCKE = Max(RU(1.75ns/tCK),4nCK)	Table 94,section 4.48.1
61	REF to PDE < tREF_PDE_CC	SR	tREF_PDE_CC = tCMDCKE = Max(RU(1.75ns/tCK),3nCK)	Table 94,section 4.48.1
62	REFA to PDE < tREFA_PDE_CC	SR	tREFA_PDE_CC = tCMDCKE = Max(RU(1.75ns/tCK),4nCK)	Table 94,section 4.48.1
63	ACT to PDE < tACT_PDE_CC	SR	tACT_PDE_CC = tCMDCKE = Max(RU(1.75ns/tCK),3nCK)	Table 94,section 4.48.1
64	MRW to PDE < tMRWCKEL_CC	SR	tMRWCKEL_CC = Max(RU(14ns/tCK), 10nCK)	Table 94

65	WR/MASK-WR to PDE < tWR_PDE_CC	SR	tWR_PDE_CC = WL + (tDQSS(Max) + RU(tDQS2DQ(Max)/tCK) + BL/2 +RU(tWR/tCK)	section 4.48.1, Fig. 139 Table 27 - tDQSS max = 1.25tCK
66	WRA/MASK-WRA to PDE < tWRA_PDE_CC	SR	tWRA_PDE_CC = WL + tDQSS(Max) + tDQS2DQ(Max) + BL/2 + nWR + (2 tCK)	section 4.36.1, Fig. 140 Table 27 - tDQSS max = 1.25tCK
67	RD/RDA to PDE < tRD_PDE_CC Subtracts 8 @ BL16 OTF[2]	SR	tRD_PDE_CC = RL + tDQSCK(Max) + BL/2 + 2tCK	Notes under Fig. 138
68	MRR to PDE < tMRR_PDE_CC MRR is always BL 16	SR	tMRR_PDE_CC = RL + tDQSCK(Max) + BL/2 + 2tCK	Notes under Fig. 144
69	Start ZQCAL to PDE < tZQCKE_CC	SR	tZQCKE_CC = tCMDCKE = Max(RU(1.75ns/tCK),3nCK)	Table 94, Figure 146 MPC to start ZQCal to PDE