

The DDR Detective®

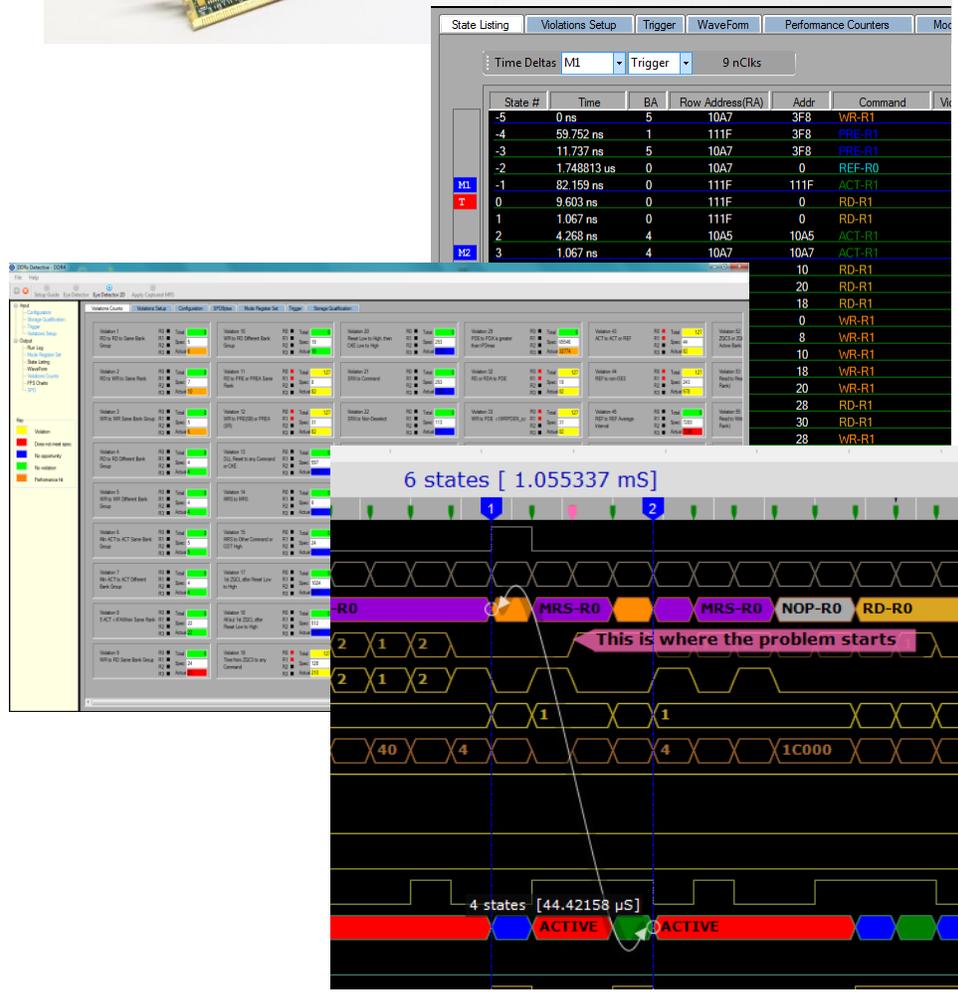
DDR Protocol, Compliance, Performance, Trace and System Characterization all in one tool!

Key Features

- Supports **DDR3** , **DDR4**, **LPDDR3** and soon **LPDDR4!**
- Thousands of counters for DDR4 count performance metrics real time *all the time*
- Analyzes bus speeds up to 2667 MT/s
- 8GB Internal memory can store up to 512M Captured States!
- Real time analysis, not only post-processing
- Eye Detector guarantees valid data acquisition
- Protocol Violation Detector executes hundreds of simultaneous real time tests
- **Row Hammer Detection** captures those unexplained DDR3 memory failures!
- Interactions among up to 8 ranks, over two slots are analyzed.
- Mode register capture is supported on up to 8 ranks, in 1 or 2 slots.
- Performance Counters, Reads, Writes, total Clocks, by rank, also power management information
- Supports Auto-Clock rate detect and clock stoppage for LPDDR3 and DDR4
- Connects to the target under test with DIMM, SO-DIMM, and BGA interposers or a midbus probe
- Integrated MicroSoft Charts gives quick insight into large trace captures



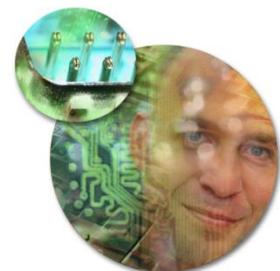
FS2800



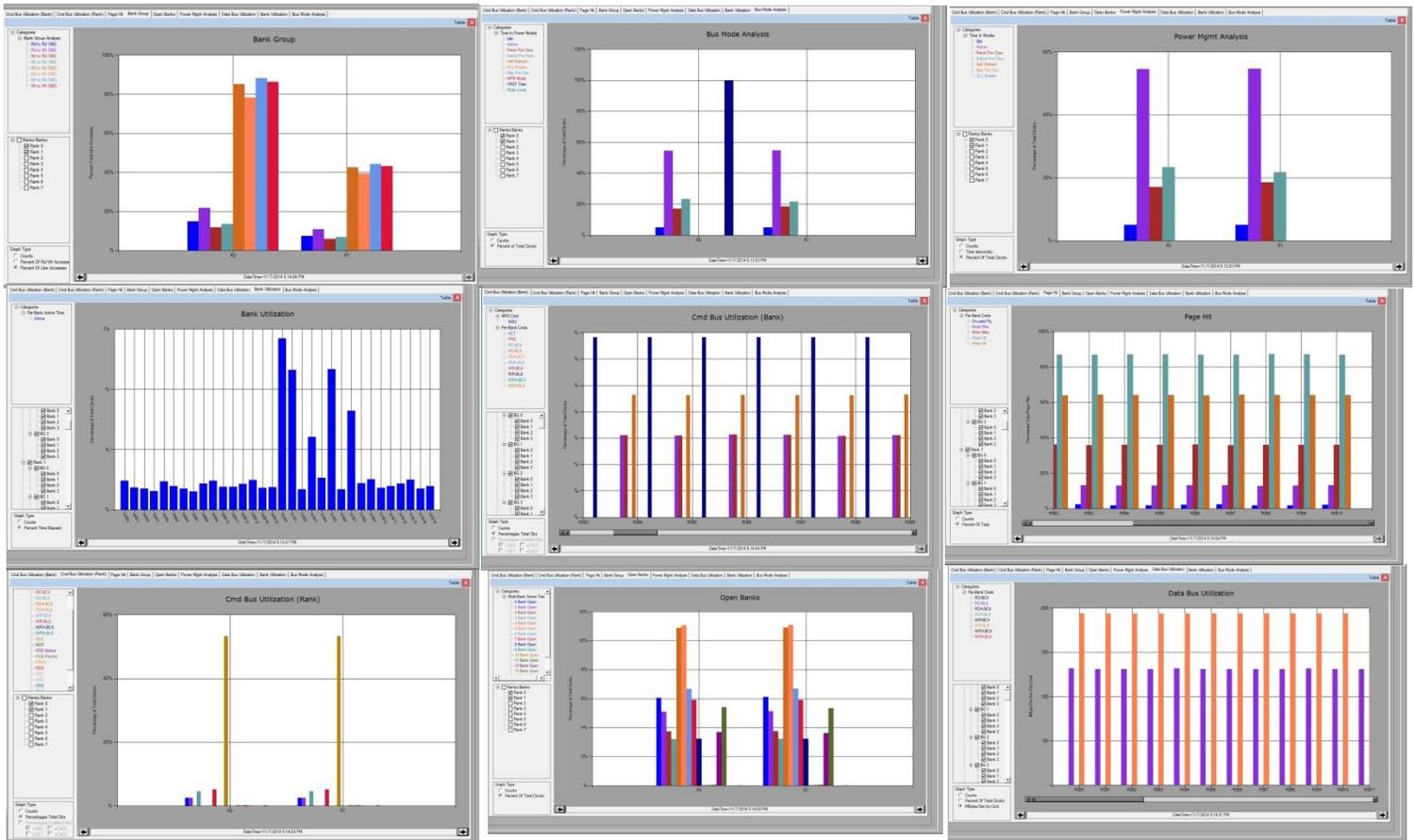
Up to 512M captured states!
Hardware Filtering (storage qualification) gives 70% more!
State Listing and State Waveform

Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our protocol, performance and power management analyzers combined with our Interposers and software help you monitor and verify complex activities on your advanced-technology computer bus design. FuturePlus Systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

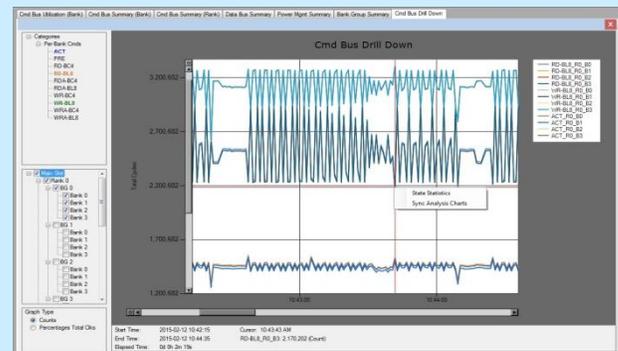


DDR4 Performance event reporting in real time *all the time* uploaded every second for as long as you have disk space!



New DDR4 Performance features

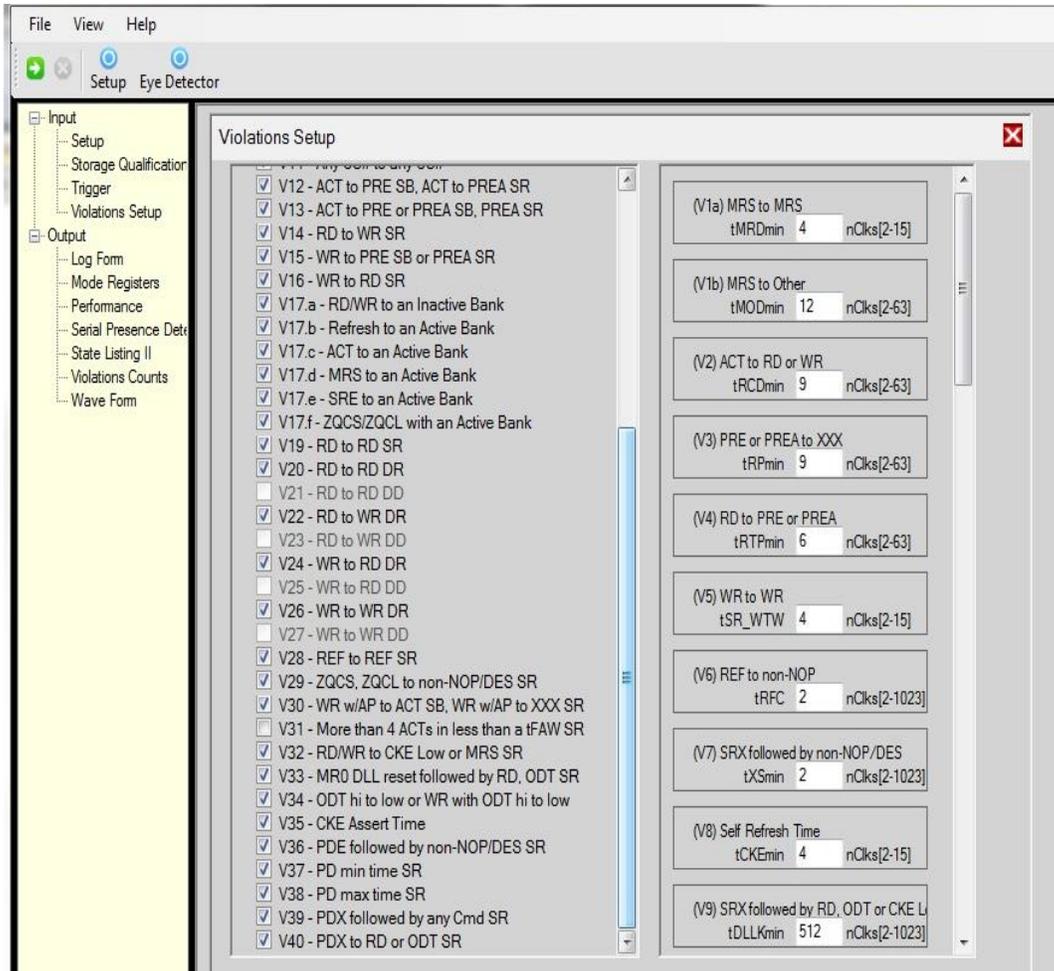
- Bus Command Utilization Analysis
- Page Hit Analysis
- Bank Group Analysis
- Power Management Analysis
- Multiple Open Bank Analysis
- Bank Utilization Analysis
- Data bus Utilization Analysis
- Bus Mode Analysis (Reset, Idle, Active, Precharge PD, Active PD, Max PD, SRX, DLL Dis, Write Leveling, MPR mode and Vref Training)
- Summary/Drill down mode shows hours and even days of results in a single view



On every clock cycle! **Real Time All The Time Continuous Analysis**
What does this mean? Currently available products capture a miniscule amount of DDR traffic, count the events in the trace and then display. Deadtime between traces and trace depth give only a small sampling of actual DDR events. The DDR Detective use new breakthrough architecture to accumulate events on EVERY cycle! Thus no bus events are missed. This never been done before feature gives unprecedented insight into DDR bus activity for validation, system architects, software engineers and designers.

The DDR Detective® Protocol Compliance

Unique Scoreboard displays errors in real time using counters not post processed information



Violation	R0	R1	R2	R3	Total
Violation 10 ACT To ACT (tRRD)	■	■	■	■	2794
Violation 11 Any CS# asserted for more than 1 cycle or CS# to any CS#	Main ■	Satellite ■	■	■	2794
Violation 12 ACT to PRE	■	■	■	■	2794
Violation 13 ACT to PRE, PEA or ACT to AP	■	■	■	■	0
Violation 14 Same rank RD to WR	■	■	■	■	0
Violation 15 WR to PRE or PEA	■	■	■	■	2794
Violation 16 Same rank WR to RD	■	■	■	■	2794
Violation 17 Active bank check(s)	■	■	■	■	2794
Violation 19 Same rank RD to RD	■	■	■	■	2794
Violation 20 Different rank RD to RD	■	■	■	■	2794

The DDR Detective® :

- Covers 65 tests on all banks and ranks for over 1000 concurrent checks
- Stored Log file lists test failure, day and time of day when the failure occurred
- Scoreboard display gives quick indication of what test is failing and on what rank
- 8Gb of trace memory has advanced Charting feature
- Auto configures the sampling window for acquisition of address, command and control for the DDR Detective and does not rely on latches that need stable clock/data relationship

Additional Protocol Probe Features:

- Automatically calculates protocol parameters based on JEDEC specifications and loads into the protocol checking function.
- Allows user to override and enter new parameter values
- Ability to enable and disable each compliance test
- Allows user to load the DDR Detective configuration or save parameters
- Monitors and displays running totals of the test failures and performance counters once per second.
- 512M states with store qualification on any command and trigger on any DDR event

Margin Testing

- Measure your memory sub-systems latencies
- Characterize memory latency performance
- Learn what how much margin your system is operating at
- See if test coverage is complete



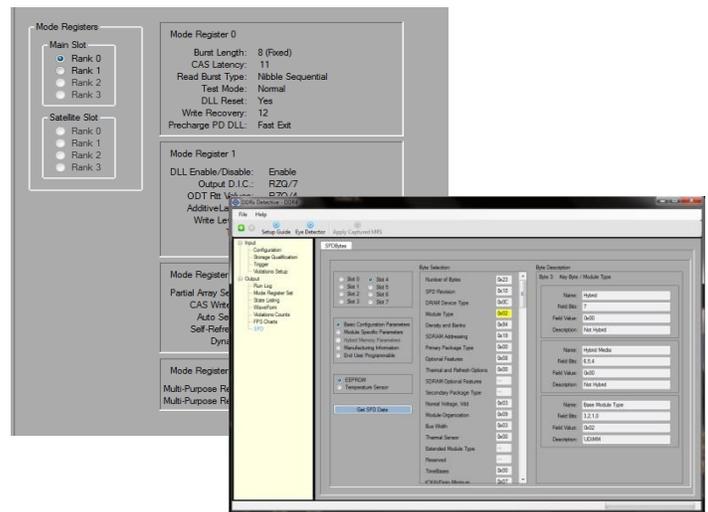
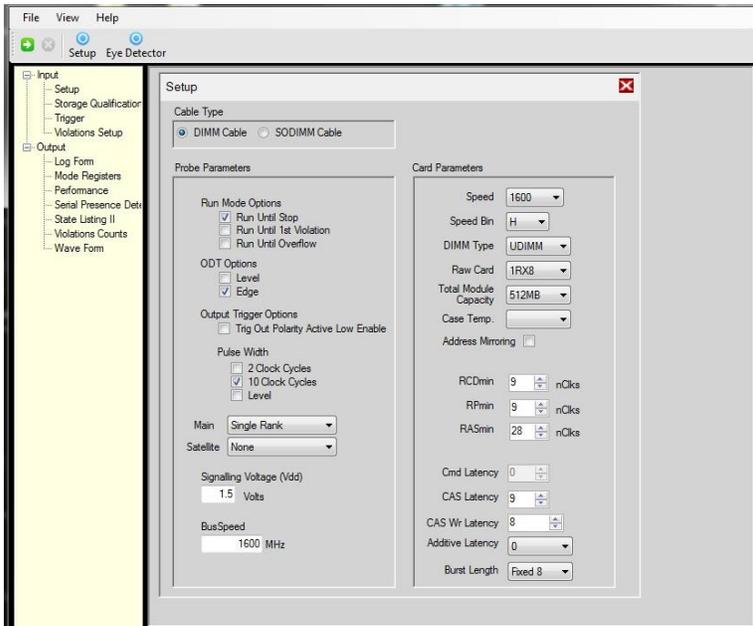
Performance Hit!
Transactions could be closer together to increase bandwidth

Event not occurring so no margin can be measured

JEDEC Spec violation!
Commands are too close together, risk data corruption

Perfect!
Operating right at specification

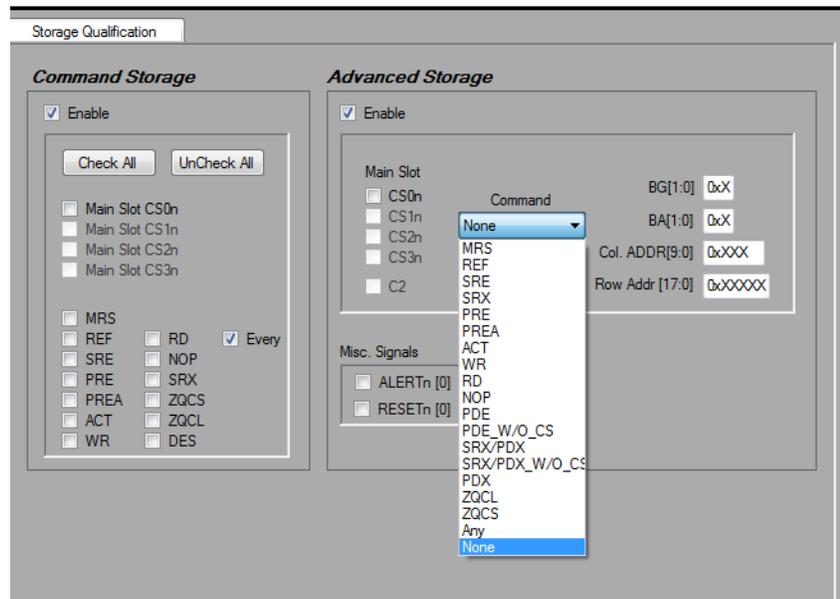
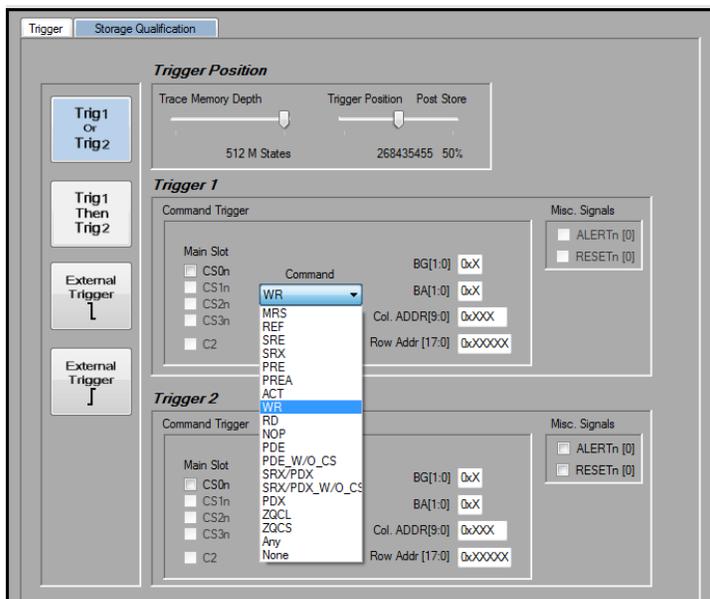
Automated Setup



- MRS Capture
- SPD Capture
- Eye Detector*

*no interposer latches allows for use in marginal systems

Easy Triggering and Storage Qualification



- Full address/command triggering in one step*
 - Use any transaction with address as a store qualifier*
 - Store only certain commands or just violations*
 - Store only Accesses to a certain bank group/bank/rank*
- * Features found only on the NEW DDR Detective

State Listing and Waveform

The FS2800 displays 512M states with Time Stamps

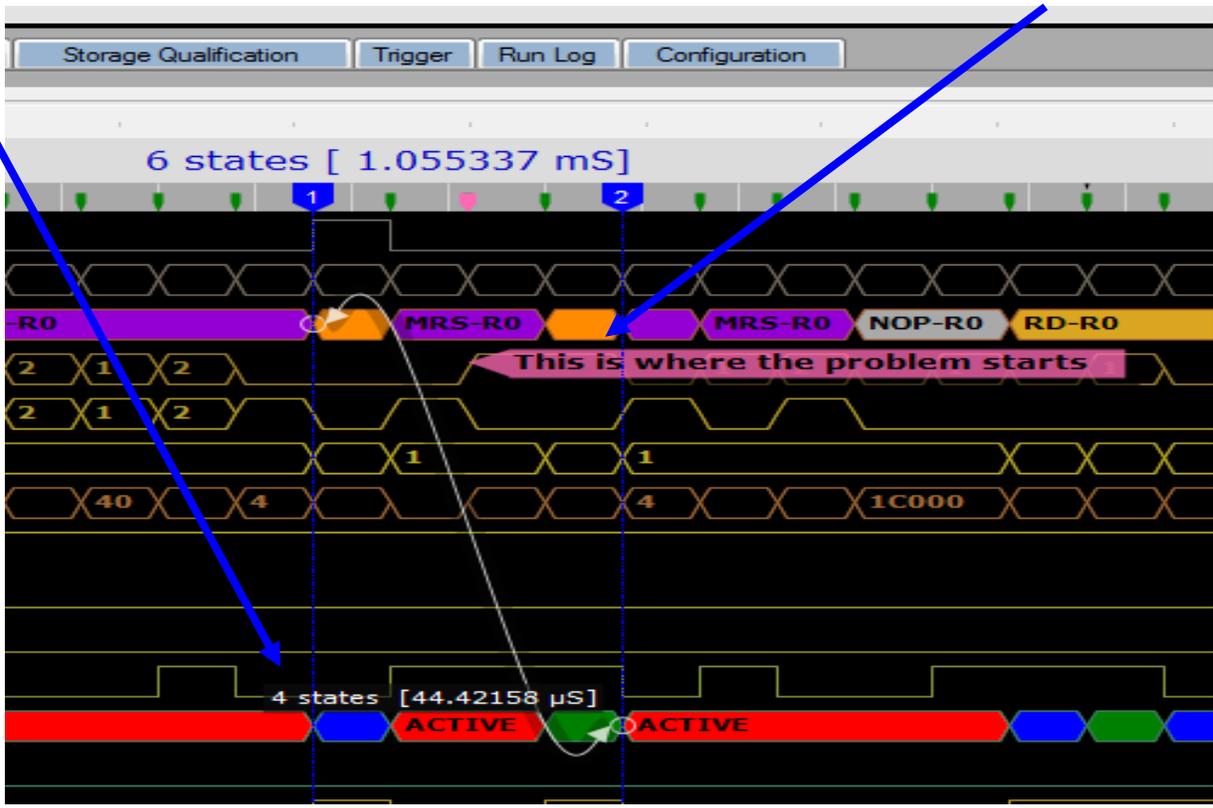
State #	Time	BA	Row Address(RA)	Addr	Command	Violation(PV)	ViolationID	CKE1	CKE0	CS3n	CS2n	CS1n	CS0n
-5	0 ns	5	10A7	3F8	WR-R1	0		1	1	1	1	1	0
-4	59.752 ns	1	111F	3F8	PRE-R1	0		1	1	1	1	1	0
-3	11.737 ns	5	10A7	3F8	PRE-R1	0		1	1	1	1	1	0
-2	1.748813 us	0	10A7	0	REF-R0	0		1	1	1	1	1	0
-1	82.159 ns	0	111F	111F	ACT-R1	0		1	1	1	1	1	0
0	9.603 ns	0	111F	0	RD-R1	1	2	1	1	1	1	1	0
1	1.067 ns	0	111F	0	RD-R1	1	2	1	1	1	1	1	0
2	4.268 ns	4	10A5	10A5	ACT-R1	0		1	1	1	1	1	0
3	1.067 ns	4	10A7	10A7	ACT-R1	1	10	1	1	1	1	1	0
4	3.201 ns	0	111F	10	RD-R1	0		1	1	1	1	1	0
5	4.268 ns	0	111F	20	RD-R1	0		1	1	1	1	1	0
6	4.268 ns	0	111F	18	RD-R1	0		1	1	1	1	1	0
7	11.737 ns	7	10A7	0	WR-R1	0		1	1	1	1	1	0
8	4.268 ns	4	10A7	8	WR-R1	0		1	1	1	1	1	0
9	4.268 ns	4	10A7	10	WR-R1	0		1	1	1	1	1	0
10	4.268 ns	4	10A7	18	WR-R1	0		1	1	1	1	1	0
11	4.268 ns	7	10A7	20	WR-R1	0		1	1	1	1	1	0
12	28.809 ns	0	111F	28	RD-R1	0		1	1	1	1	1	0
13	4.268 ns	0	111F	30	RD-R1	0		1	1	1	1	1	0
14	11.737 ns	4	10A7	28	WR-R1	0		1	1	1	1	1	0
15	4.268 ns	4	10A7	0	WR-R1	0		1	1	1	1	1	0
16	23.474 ns	7	10A7	30	PRE-R1	0		1	1	1	1	1	0
17	33.077 ns	0	111F	30	PRE-R1	0		1	1	1	1	1	0
18	13.871 ns	0	111F	111F	ACT-R1	0		1	1	1	1	1	0
19	2.134 ns	4	10A7	111F	PRE-R1	0		1	1	1	1	1	0
20	7.469 ns	0	111F	40	RD-R1	1	2	1	1	1	1	1	0
21	1.067 ns	0	111F	40	RD-R1	1	2	1	1	1	1	1	0
22	4.268 ns	4	10A7	10A5	ACT-R1	0		1	1	1	1	1	0
23	1.067 ns	4	10A7	10A7	ACT-R1	1	10	1	1	1	1	1	0
24	10.67 ns	7	10A7	40	WR-R1	1	17a	1	1	1	1	1	0
25	4.268 ns	4	10A7	38	WR-R1	0		1	1	1	1	1	0
26	57.618 ns	0	111F	48	RD-R1	0		1	1	1	1	1	0

Tool tracks Rank Power Status a metric only found in the FS2800!

HW store qualification stores only transactions of interest

Shows the violation on the exact state it occurs on.

Innovative State Waveform lets you add markings and notes to the waveform display



Row Hammer Detection

DDR3 memory is plagued by a known failure mechanism called Row Hammer. See an informative video here: [Row Hammer explained](#). A white paper on the topic can be found [here](#).

Row Hammer Detection feature for DDR3

- Tracks and counts every ACTIVATE command
- Indicates if thresholds are crossed
- Output displays rank and bank of rows that show excessive ACTIVATE commands
- Exact Row Address indicated
- Address Range feature makes Row Hammer Detection even more accurate!
- Helps find those unexplained memory errors!
- [See a video of this tool in action](#)

The screenshot displays the DDR3 Row Hammer Detection tool interface. The main window is titled "DDR3 Detective - DDR3 Row Hammer Mode". It features a "Row Hammer Setup" tab and a "Row Hammer" tab. The "Row Hammer Setup" tab includes a "Configuration" section with a "Row Hammer" sub-section where the "Enable" checkbox is checked. The "Address Range" section shows "Upper Address Limit" and "Lower Address Limit" fields. The "Data Parameters" section includes "Data Display Parameters" and "Data Report Parameters". The "Threshold Limits" section shows "Threshold 1" and "Threshold 2" fields. The "Row Hammer" tab displays a heatmap of row hammer activity across 8 banks (Bank 0 to Bank 7) and 4 ranks (Rank 0 to Rank 3). The heatmap shows activity in Bank 2, Bank 3, and Bank 4. A "Data Packets" list shows the following data:

```
T1U0: Rank: 0 Bank: 2 RA: 3F6E
T2U0: Rank: 0 Bank: 2 RA: 3F6E
T1U0: Rank: 0 Bank: 2 RA: 35E2
T1U0: Rank: 0 Bank: 3 RA: 35E2
T1U0: Rank: 0 Bank: 0 RA: 35E2
T1U0: Rank: 0 Bank: 1 RA: 35E2
T1U0: Rank: 0 Bank: 3 RA: 35E3
T1U0: Rank: 0 Bank: 2 RA: 35E3
T1U0: Rank: 0 Bank: 1 RA: 35E3
T1U0: Rank: 0 Bank: 0 RA: 35E3
T1U0: Rank: 0 Bank: 0 RA: 35E4
T1U0: Rank: 0 Bank: 1 RA: 35E4
T1U0: Rank: 0 Bank: 2 RA: 3F6E
T2U1: Rank: 0 Bank: 2 RA: 3F6E
T1U0: Rank: 0 Bank: 1 RA: 35E5
T1U1: Rank: 0 Bank: 1 RA: 35E5
T1U1: Rank: 0 Bank: 0 RA: 35E5
T1U0: Rank: 0 Bank: 0 RA: 35E5
T1U0: Rank: 0 Bank: 3 RA: 35E5
T1U1: Rank: 0 Bank: 3 RA: 35E5
T1U1: Rank: 0 Bank: 0 RA: 35E6
T1U0: Rank: 0 Bank: 3 RA: 35E6
T1U1: Rank: 0 Bank: 0 RA: 35E6
T1U0: Rank: 0 Bank: 3 RA: 35E6
T1U0: Rank: 0 Bank: 1 RA: 35E6
T1U1: Rank: 0 Bank: 1 RA: 35E7
T1U0: Rank: 0 Bank: 2 RA: 35E7
T1U0: Rank: 0 Bank: 2 RA: 3F6E
T1U0: Rank: 0 Bank: 1 RA: 35E7
```

The "Run Log Output" section shows the following log entries:

```
Time value="6/6/2014 11:02:24 AM" />
Threshold thresholdID_1="30" Rank="1" Bank="1" RowAddress="3F6C" />
Time value="6/6/2014 11:02:25 AM" />
Threshold thresholdID_1="31" Rank="1" Bank="1" RowAddress="3F6C" />
Time value="6/6/2014 11:02:26 AM" />
Threshold thresholdID_1="32" Rank="1" Bank="1" RowAddress="3F6C" />
Time value="6/6/2014 11:02:27 AM" />
Threshold thresholdID_1="32" Rank="1" Bank="1" RowAddress="3F6C" />
Time value="6/6/2014 11:02:28 AM" />
Threshold thresholdID_1="31" Rank="1" Bank="1" RowAddress="3F6C" />
Time value="6/6/2014 11:02:29 AM" />
Threshold thresholdID_1="32" Rank="1" Bank="1" RowAddress="3F6C" />
```

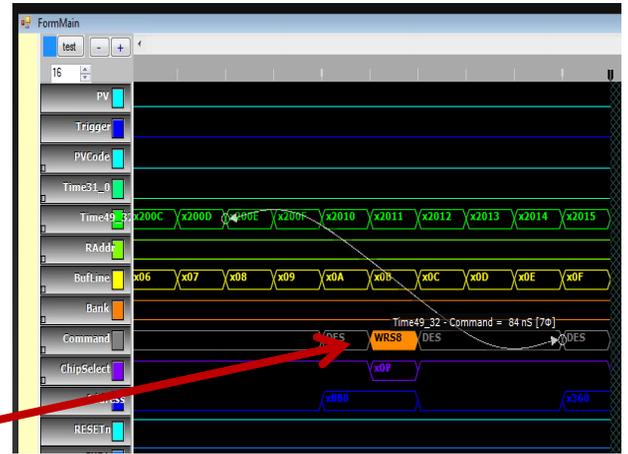
The "Legend" section shows the following thresholds:

- T1 Threshold: 1000
- T2 Threshold: 10000

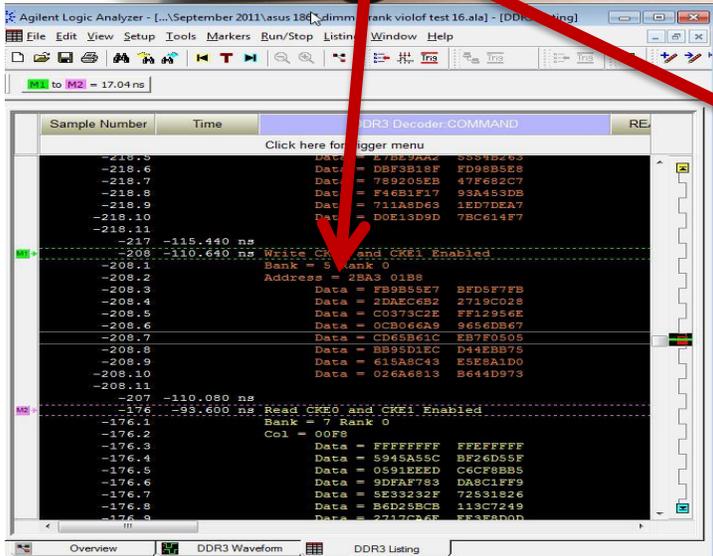
The "Total Run Time" is 8 seconds. The "Data Packets" list is sorted by Time. The "Run Log Output" is sorted by Time. The "Data Packets" list is sorted by Time. The "Run Log Output" is sorted by Time.

Trigger out to Logic Analyzer or scope

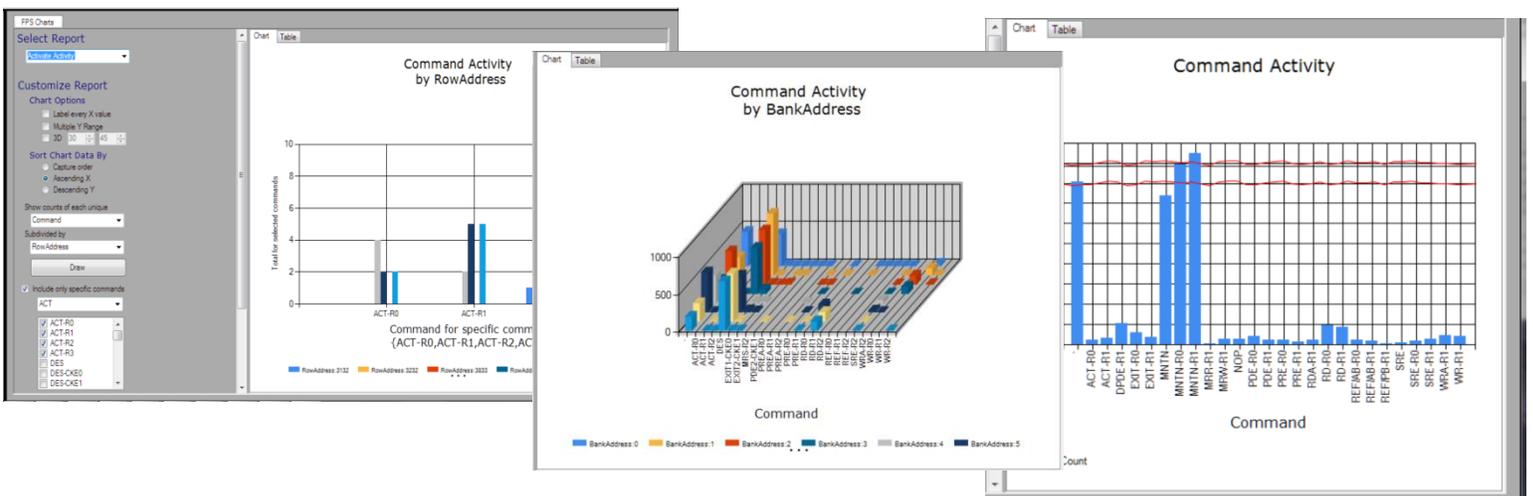
State #	Time	BA	Row Address(RA)	Addr	Command	Violation(PV)	ViolationID
-5	0 ns	5	10A7	3F8	WR-R1	0	
-4	59.752 ns	1	111F	3F8	PRE-R1	0	
-3	11.737 ns	5	10A7	3F8	PRE-R1	0	
-2	1.748813 us	0	10A7	0	REF-R0	0	
-1	82.159 ns	0	111F	111F	ACT-R1	0	
0	9.603 ns	0	111F	0	RD-R1	1	2
1	1.067 ns	0	111F	0	RD-R1	1	2
2	4.268 ns	4	10A5	10A5	ACT-R1	0	
3	1.067 ns	4	10A7	10A7	ACT-R1	1	
4	3.201 ns	0	111F	10	RD-R1	0	
5	4.268 ns	0	111F	20	RD-R1	0	
6	4.268 ns	0	111F	18	RD-R1	0	



Find Problems Faster!

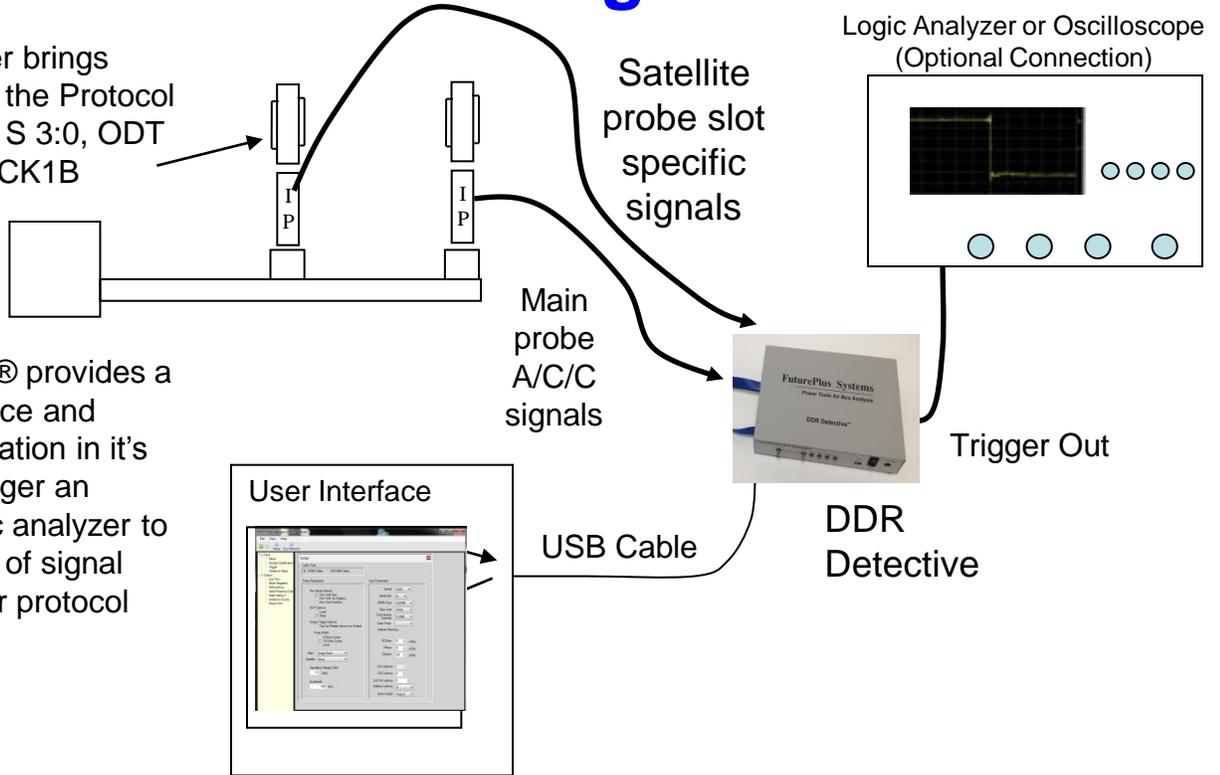


Charting feature quickly sorts stored data



Functional Diagram

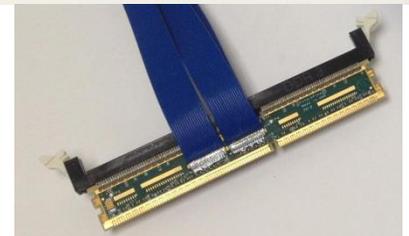
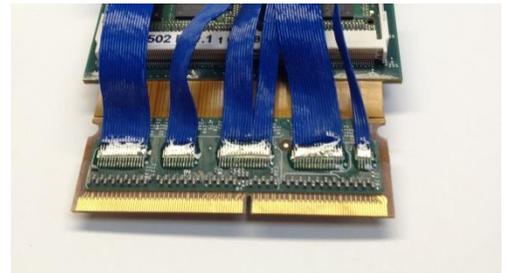
The satellite interposer brings second slot signals to the Protocol Probe logic: CKE 1:0, S 3:0, ODT 1:0, CK0/CK0B, CK1/CK1B



The DDR Detective® provides a rich set of Compliance and Performance information in its display, and can trigger an oscilloscope or logic analyzer to give a detailed view of signal integrity problems or protocol errors.

Connecting to the Target

- DIMM and SODIMM Interposers
- BGA Interposers
- MidBus Footprint
- DIMM and SODIMM interposers that also connect to the Logic Analyzer for full DQ/DQS trace



Ordering Information

- FS2800 DDR3/DDR4 Trace DDR Detective
FS2821 Add FS2801 LPDDR3 functionality to the FS2800
- FS2820 Add DDR4 Violation Detection to DDR Detective
FS2850 Add DDR4 Performance Counters to DDR Detective
- FS2801 LPDDR3 DDR Detective
FS2851 ADD FS2800 DDR3/DDR4 Trace to the FS2801

Probing Options

- FS2363 Add DDR3 DIMM A/C/C Interposer for DDR Detective
FS2424 Add DDR3 SO-DIMM A/C/C Interposer for DDR Detective
FS2367 Add DDR3 DIMM Satellite* Interposer for DDR Detective
FS2422 Add DDR3 SO-DIMM Satellite* Interposer for DDR Detective
- FS2823 Add DDR4 DIMM A/C/C Interposer for DDR Detective
FS2824 Add DDR4 SO-DIMM A/C/C Interposer for DDR Detective
FS2853 Add DDR4 DIMM Satellite* Interposer for DDR Detective
FS2854 Add DDR4 SO-DIMM Satellite* Interposer for DDR Detective
- FS2826 Add DDR Midbus A/C/C Connection for DDR Detective
- FS2425 DDR3 BGA Cable Adapter and SW upgrade to support BGA
FS2852 DDR4 BGA Cable Adapter and SW upgrade to support BGA

Probing Options that include Logic Analyzer connections

- FS2362 DDR3 2400 DIMM Interposer A/C/C/DQ for the FS280x/U4154A
FS2436 DDR3 SO-DIMM Interposer A/C/C/DQ for the FS280x and LA
FS2835 DDR4 DIMM Interposer A/C/C/DQ for the FS280x/U4154A
FS2836 DDR4 SO-DIMM Interposer A/C/C/DQ for the FS280x/U4154A

* Satellite gives Slot 2 Probing for same channel

See <http://www.futureplus.com/products> for detailed requirements.

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KEYSIGHT
TECHNOLOGIES

Strategic Solutions Partner

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