JEDEC

Global Standards for the Microelectronics Industry

# Google Study:

## Could those memory failures be caused by design flaws?

Barbara P. Aichinger
Vice President New Business Development
FuturePlus Systems Corporation
www.FuturePlus.com
Barb.Aichinger@FuturePlus.com

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# What was the Google Study?

- DRAM Errors in the Wild: A Large-Scale Field Study Schroeder,Pinheiro,Weber;SIGMETRICS/Performance '09 June
- This study tried to make sense of memory failures in Google's fleet of servers
  - Concluded that failures were orders of magnitude more prevalent than advertised
  - No specific conclusion could be reached as to the source of the errors
  - Noted that some failures followed the server versus the memory

# Additional Conclusions

- 1.3% was the average Uncorrectable error rate across the fleet per year
  - Some platforms experienced 2-4% error rate per year
- Temperature had a small effect on error rate
- Newer Generation DIMMs did not show worse error rates as commonly feared (DDR1,DDR2 and FBDIMM)

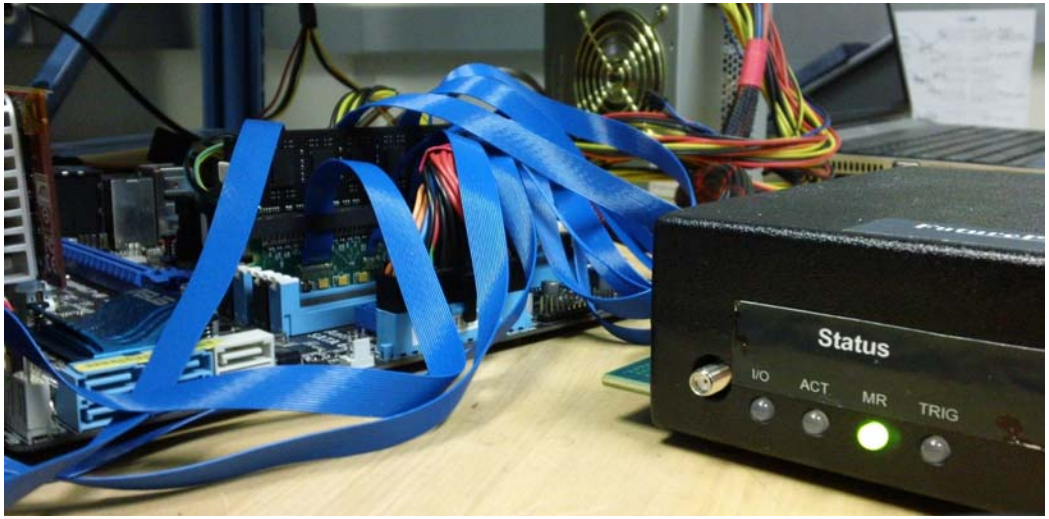
# A Paradigm Shift for Memory Compliance Testing

- The Google Study did not have the advantage of the new tools that can automate Protocol Compliance Testing *In The Wild*
- Their conclusions could not find the source of the unexpectedly high error rate
- Improvement in error rates is critical to industries that rely upon large fleets of Servers

# What is Protocol Compliance?

- Correct Timing between events on the DDR memory bus
- DDR3 Example:
  - Read operation followed by a Precharge
  - Write command followed too quickly by a Read command
  - Average Refresh rate

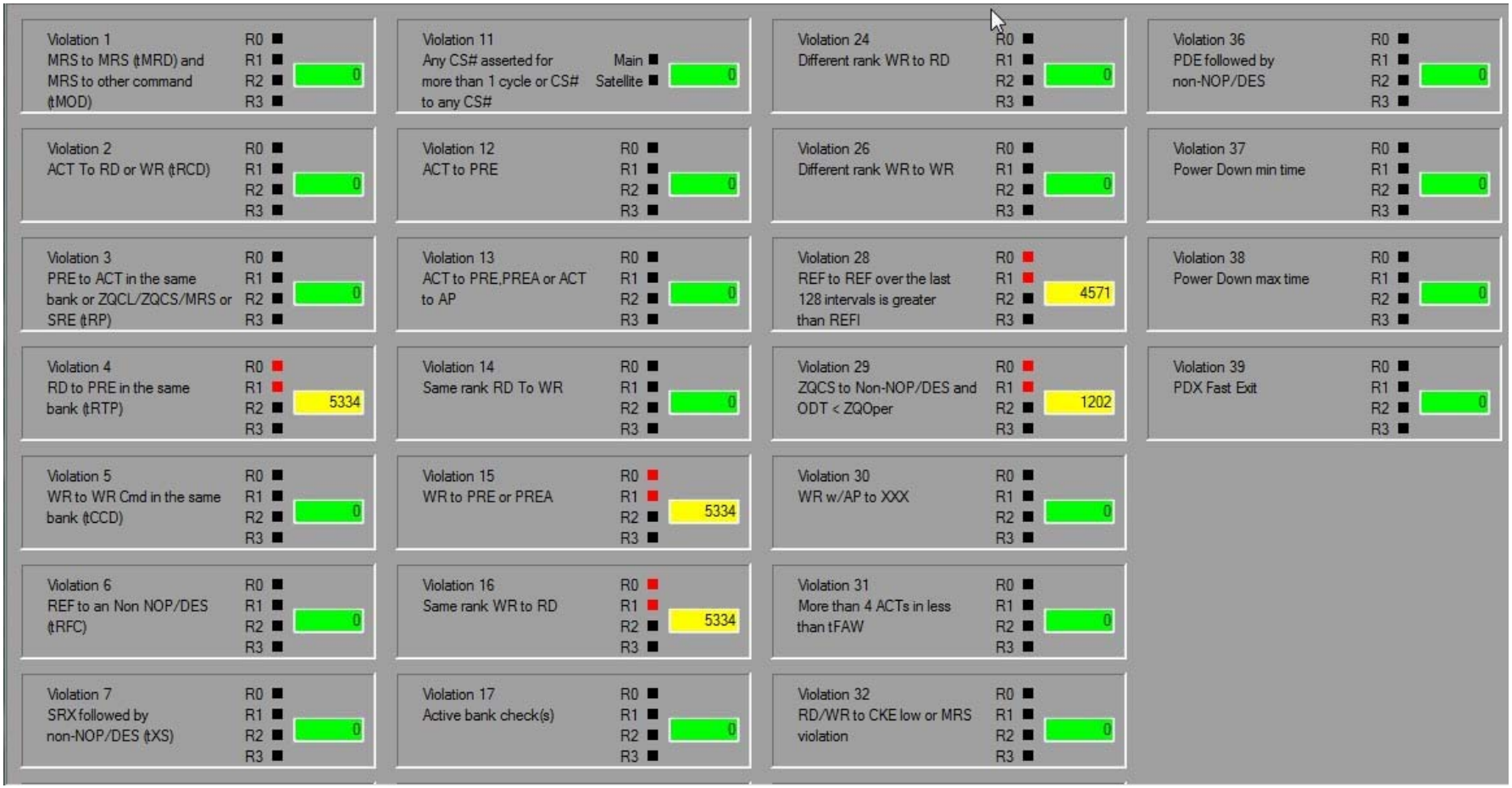
# Our Study



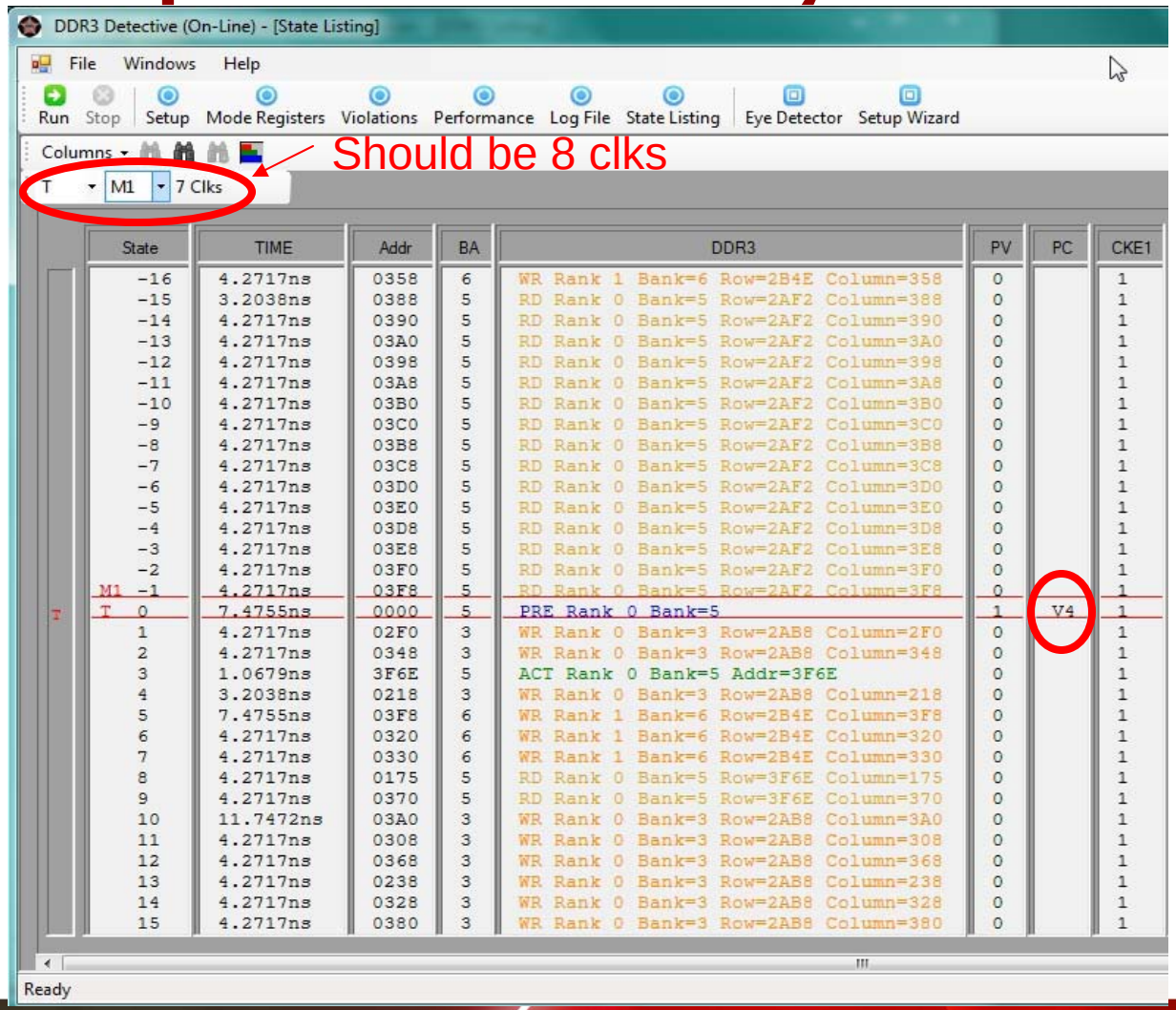


- Commercially available motherboards
- FuturePlus Systems DDR3 Detective™
- DIMMs and a FuturePlus DIMM interposer

# Examples of Protocol Compliance Failures



# A READ to PRECHARGE Rank 0 Bank 5 separation fails by 1 clock

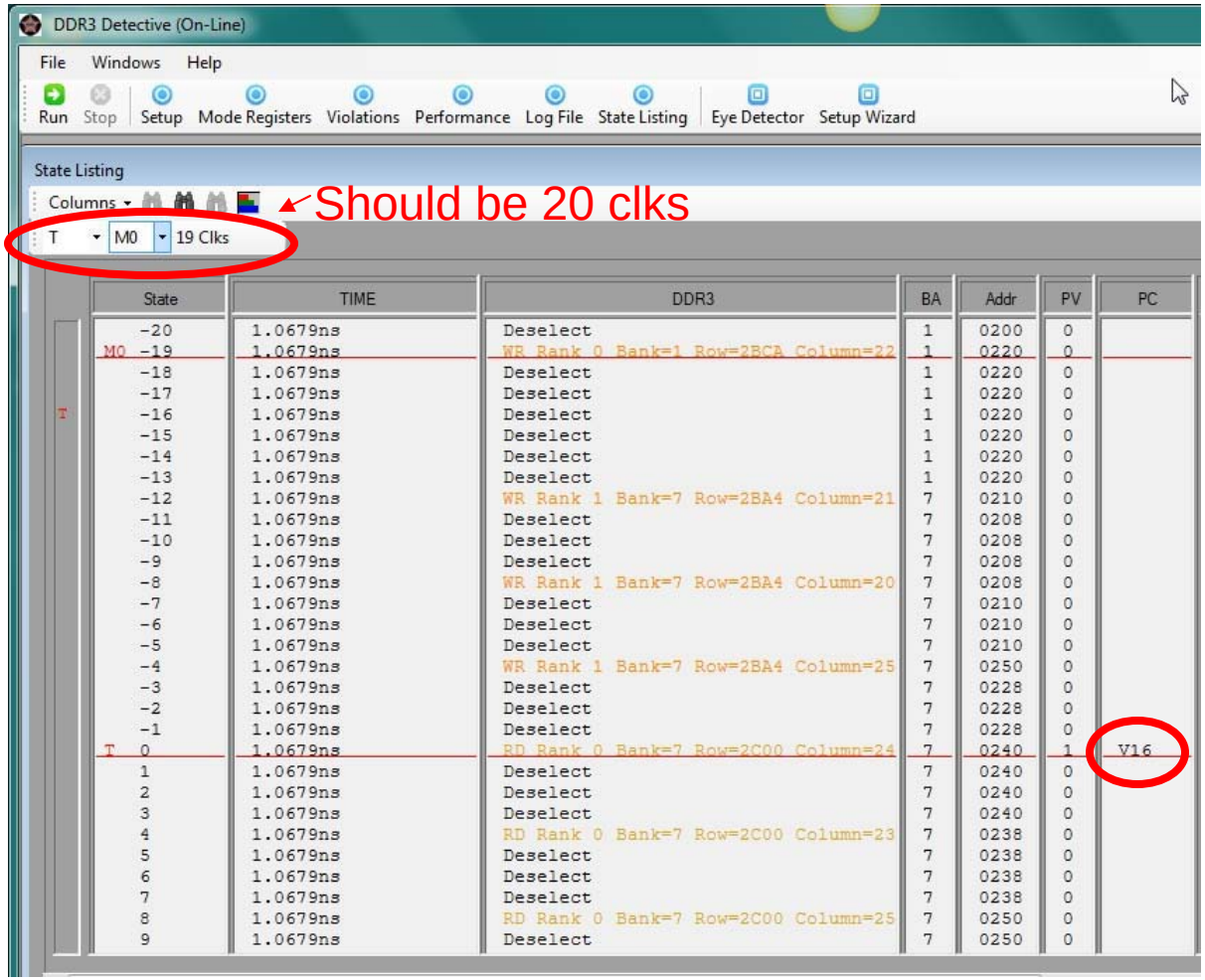



| State | TIME | Addr | BA | DDR3 | PV | PC | CKE1 |
|---|---|---|---|---|---|---|---|
| -16 | 4.2717ns | 0358 | 6 | WR Rank 1 Bank=6 Row=2B4E Column=358 | 0 | | 1 |
| -15 | 3.2038ns | 0388 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=388 | 0 | | 1 |
| -14 | 4.2717ns | 0390 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=390 | 0 | | 1 |
| -13 | 4.2717ns | 03A0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3A0 | 0 | | 1 |
| -12 | 4.2717ns | 0398 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=398 | 0 | | 1 |
| -11 | 4.2717ns | 03A8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3A8 | 0 | | 1 |
| -10 | 4.2717ns | 03B0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3B0 | 0 | | 1 |
| -9 | 4.2717ns | 03C0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3C0 | 0 | | 1 |
| -8 | 4.2717ns | 03B8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3B8 | 0 | | 1 |
| -7 | 4.2717ns | 03C8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3C8 | 0 | | 1 |
| -6 | 4.2717ns | 03D0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3D0 | 0 | | 1 |
| -5 | 4.2717ns | 03E0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3E0 | 0 | | 1 |
| -4 | 4.2717ns | 03D8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3D8 | 0 | | 1 |
| -3 | 4.2717ns | 03E8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3E8 | 0 | | 1 |
| -2 | 4.2717ns | 03F0 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3F0 | 0 | | 1 |
| M1 -1 | 4.2717ns | 03F8 | 5 | RD Rank 0 Bank=5 Row=2AF2 Column=3F8 | 0 | | 1 |
| T 0 | 7.4755ns | 0000 | 5 | PRE Rank 0 Bank=5 | 1 | V4 | 1 |
| 1 | 4.2717ns | 02F0 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=2F0 | 0 | | 1 |
| 2 | 4.2717ns | 0348 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=348 | 0 | | 1 |
| 3 | 1.0679ns | 3F6E | 5 | ACT Rank 0 Bank=5 Addr=3F6E | 0 | | 1 |
| 4 | 3.2038ns | 0218 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=218 | 0 | | 1 |
| 5 | 7.4755ns | 03F8 | 6 | WR Rank 1 Bank=6 Row=2B4E Column=3F8 | 0 | | 1 |
| 6 | 4.2717ns | 0320 | 6 | WR Rank 1 Bank=6 Row=2B4E Column=320 | 0 | | 1 |
| 7 | 4.2717ns | 0330 | 6 | WR Rank 1 Bank=6 Row=2B4E Column=330 | 0 | | 1 |
| 8 | 4.2717ns | 0175 | 5 | RD Rank 0 Bank=5 Row=3F6E Column=175 | 0 | | 1 |
| 9 | 4.2717ns | 0370 | 5 | RD Rank 0 Bank=5 Row=3F6E Column=370 | 0 | | 1 |
| 10 | 11.7472ns | 03A0 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=3A0 | 0 | | 1 |
| 11 | 4.2717ns | 0308 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=308 | 0 | | 1 |
| 12 | 4.2717ns | 0368 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=368 | 0 | | 1 |
| 13 | 4.2717ns | 0238 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=238 | 0 | | 1 |
| 14 | 4.2717ns | 0328 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=328 | 0 | | 1 |
| 15 | 4.2717ns | 0380 | 3 | WR Rank 0 Bank=3 Row=2AB8 Column=380 | 0 | | 1 |

# How critical is this failure?

- A Precharge closes a bank
- Read latency dictates when the data is to be returned
- Command telling the bank to close could be coincident with the data being returned from the bank

# Write followed too quickly by a Read to the same RANK

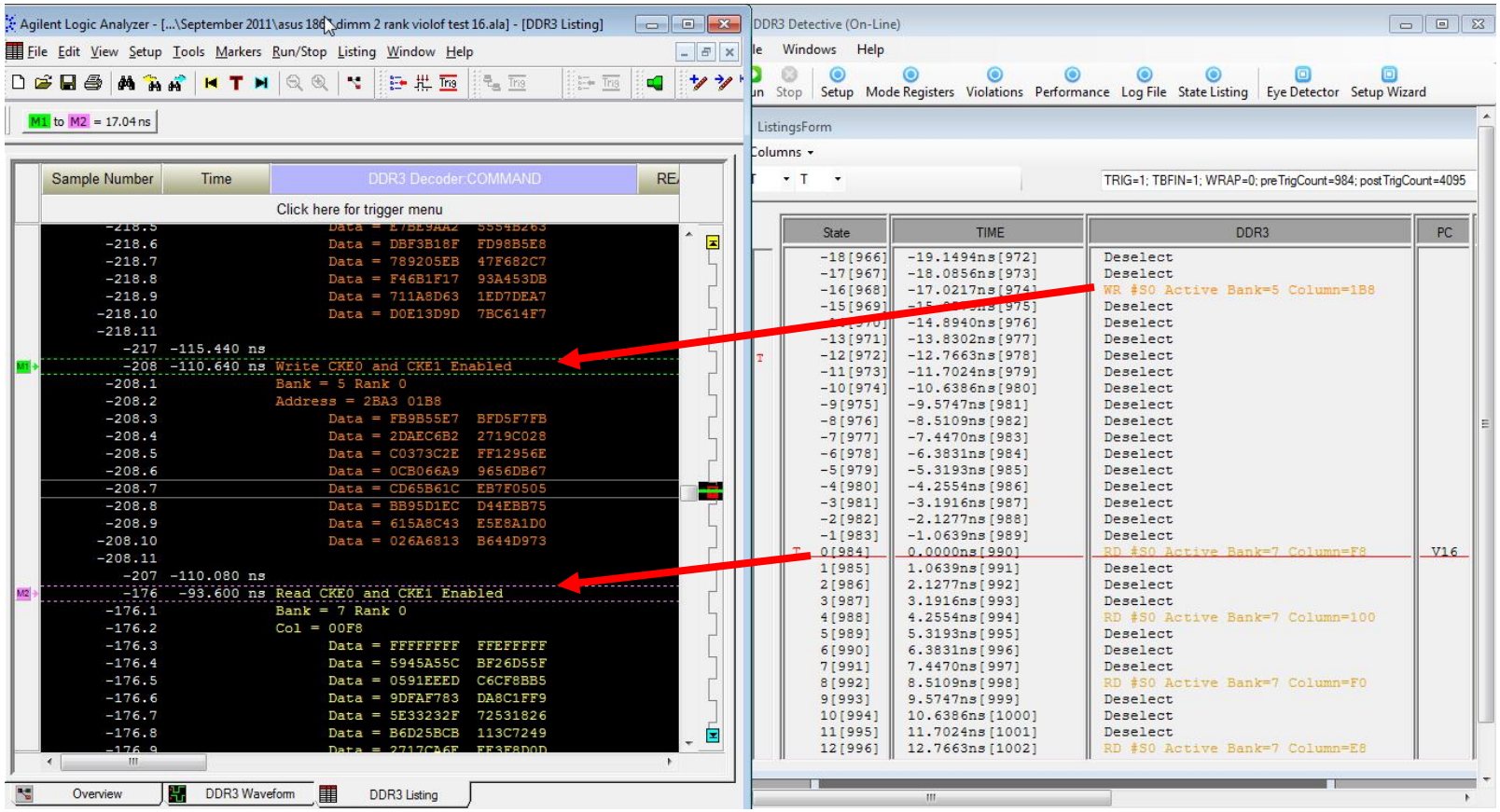



| | State | TIME | DDR3 | BA | Addr | PV | PC |
|---|---|---|---|---|---|---|---|
| | -20 | 1.0679ns | Deselect | 1 | 0200 | 0 | |
| M0 | -19 | 1.0679ns | WR Rank 0 Bank=1 Row=2BCA Column=22 | 1 | 0220 | 0 | |
| | -18 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| | -17 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| T | -16 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| | -15 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| | -14 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| | -13 | 1.0679ns | Deselect | 1 | 0220 | 0 | |
| | -12 | 1.0679ns | WR Rank 1 Bank=7 Row=2BA4 Column=21 | 7 | 0210 | 0 | |
| | -11 | 1.0679ns | Deselect | 7 | 0208 | 0 | |
| | -10 | 1.0679ns | Deselect | 7 | 0208 | 0 | |
| | -9 | 1.0679ns | Deselect | 7 | 0208 | 0 | |
| | -8 | 1.0679ns | WR Rank 1 Bank=7 Row=2BA4 Column=20 | 7 | 0208 | 0 | |
| | -7 | 1.0679ns | Deselect | 7 | 0210 | 0 | |
| | -6 | 1.0679ns | Deselect | 7 | 0210 | 0 | |
| | -5 | 1.0679ns | Deselect | 7 | 0210 | 0 | |
| | -4 | 1.0679ns | WR Rank 1 Bank=7 Row=2BA4 Column=25 | 7 | 0250 | 0 | |
| | -3 | 1.0679ns | Deselect | 7 | 0228 | 0 | |
| | -2 | 1.0679ns | Deselect | 7 | 0228 | 0 | |
| | -1 | 1.0679ns | Deselect | 7 | 0228 | 0 | |
| T | 0 | 1.0679ns | RD Rank 0 Bank=7 Row=2C00 Column=24 | 7 | 0240 | 1 | V16 |
| | 1 | 1.0679ns | Deselect | 7 | 0240 | 0 | |
| | 2 | 1.0679ns | Deselect | 7 | 0240 | 0 | |
| | 3 | 1.0679ns | Deselect | 7 | 0240 | 0 | |
| | 4 | 1.0679ns | RD Rank 0 Bank=7 Row=2C00 Column=23 | 7 | 0238 | 0 | |
| | 5 | 1.0679ns | Deselect | 7 | 0238 | 0 | |
| | 6 | 1.0679ns | Deselect | 7 | 0238 | 0 | |
| | 7 | 1.0679ns | Deselect | 7 | 0238 | 0 | |
| | 8 | 1.0679ns | RD Rank 0 Bank=7 Row=2C00 Column=25 | 7 | 0250 | 0 | |
| | 9 | 1.0679ns | Deselect | 7 | 0250 | 0 | |

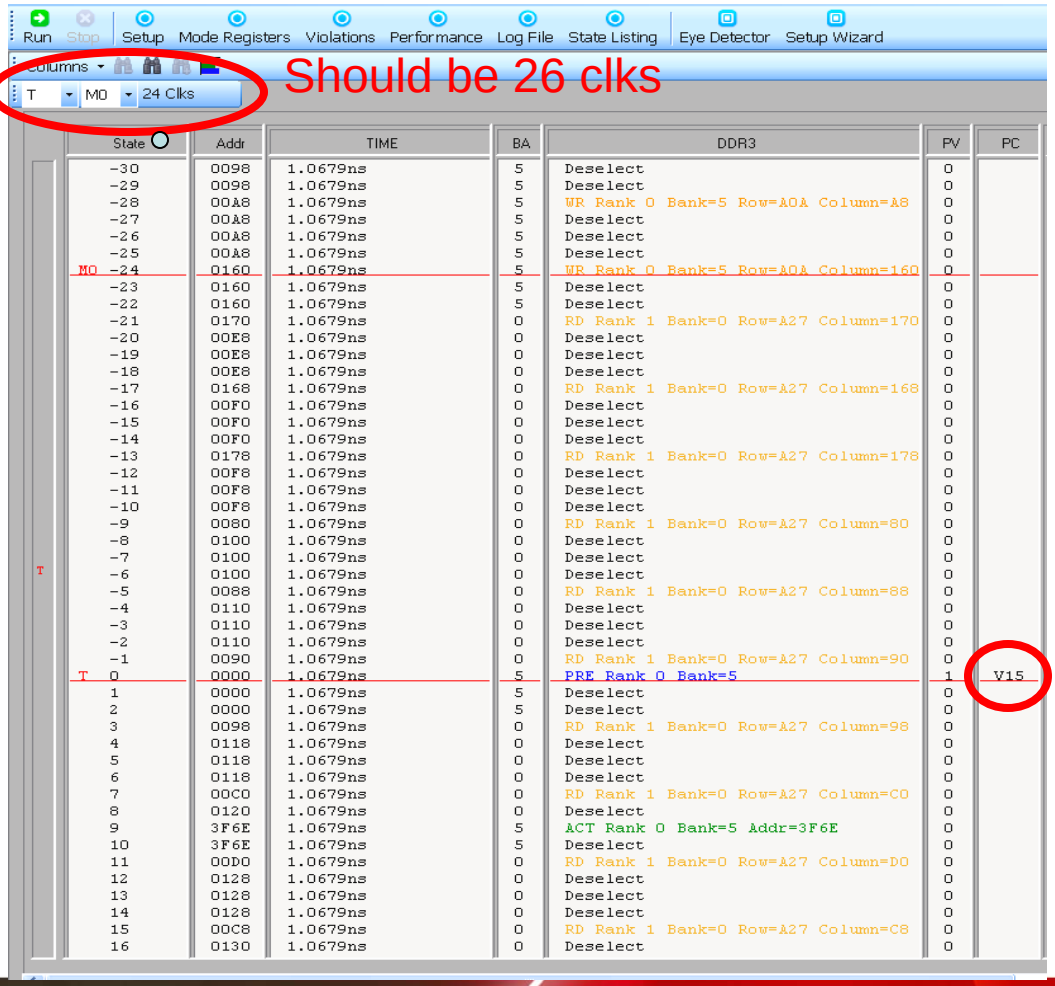
# How critical is this failure?

- The parameters for the separation of the Write and the Read are based on the latencies
- The Data bus is shared and overlapping events can lead to data corruption

# Data Corruption?



# A Write command followed too closely by a Precharge to the same bank

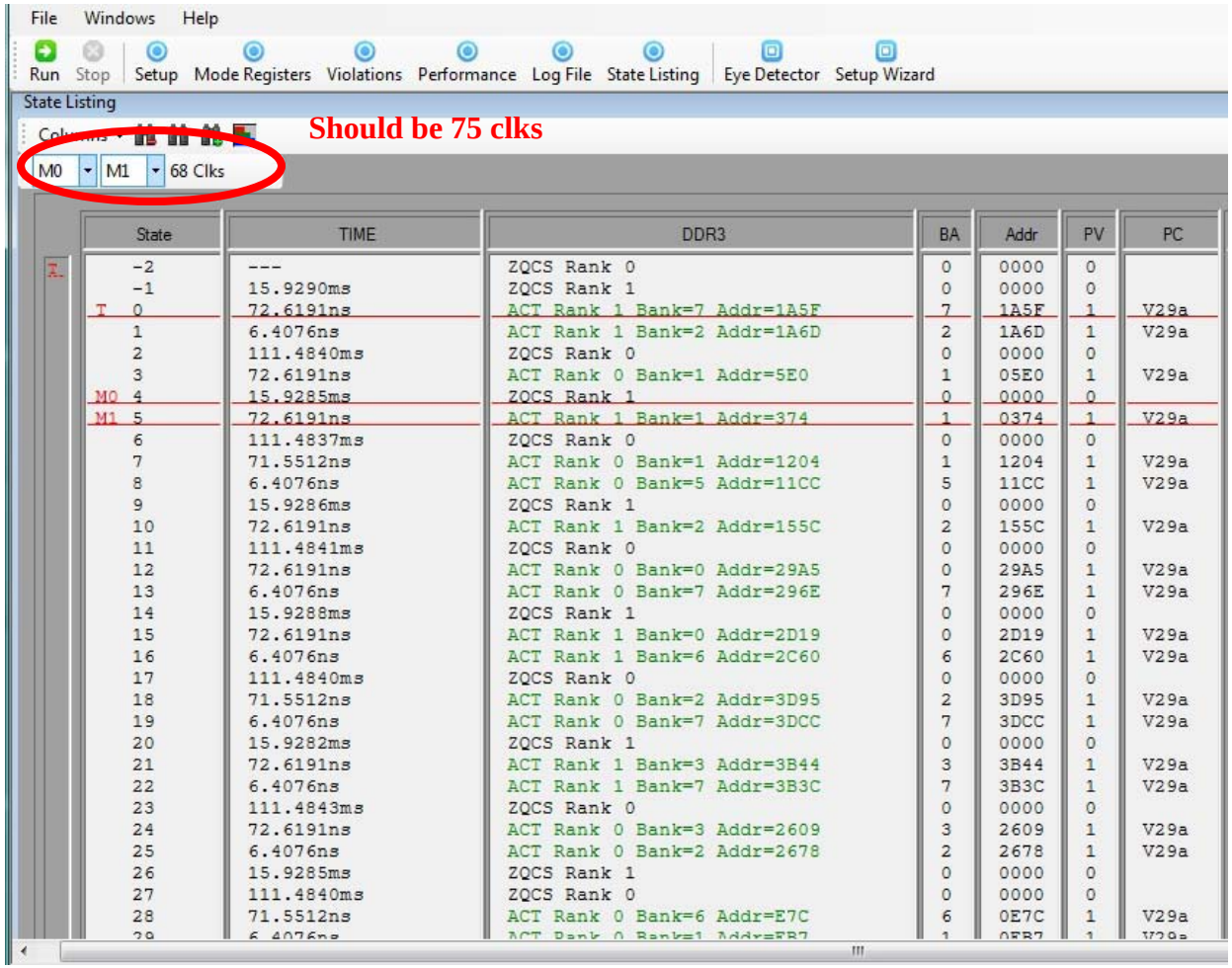



| | State | Addr | TIME | BA | DDR3 | PV | PC |
|---|---|---|---|---|---|---|---|
| | -30 | 0098 | 1.0679ns | 5 | Deselect | 0 | |
| | -29 | 0098 | 1.0679ns | 5 | Deselect | 0 | |
| | -28 | 00A8 | 1.0679ns | 5 | WR Rank 0 Bank=5 Row=A0A Column=A8 | 0 | |
| | -27 | 00A8 | 1.0679ns | 5 | Deselect | 0 | |
| | -26 | 00A8 | 1.0679ns | 5 | Deselect | 0 | |
| | -25 | 00A8 | 1.0679ns | 5 | Deselect | 0 | |
| M0 | -24 | 0160 | 1.0679ns | 5 | WR Rank 0 Bank=5 Row=A0A Column=160 | 0 | |
| | -23 | 0160 | 1.0679ns | 5 | Deselect | 0 | |
| | -22 | 0160 | 1.0679ns | 5 | Deselect | 0 | |
| | -21 | 0170 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=170 | 0 | |
| | -20 | 00E8 | 1.0679ns | 0 | Deselect | 0 | |
| | -19 | 00E8 | 1.0679ns | 0 | Deselect | 0 | |
| | -18 | 00E8 | 1.0679ns | 0 | Deselect | 0 | |
| | -17 | 0168 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=168 | 0 | |
| | -16 | 00F0 | 1.0679ns | 0 | Deselect | 0 | |
| | -15 | 00F0 | 1.0679ns | 0 | Deselect | 0 | |
| | -14 | 00F0 | 1.0679ns | 0 | Deselect | 0 | |
| | -13 | 0178 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=178 | 0 | |
| | -12 | 00F8 | 1.0679ns | 0 | Deselect | 0 | |
| | -11 | 00F8 | 1.0679ns | 0 | Deselect | 0 | |
| | -10 | 00F8 | 1.0679ns | 0 | Deselect | 0 | |
| | -9 | 0080 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=80 | 0 | |
| | -8 | 0100 | 1.0679ns | 0 | Deselect | 0 | |
| | -7 | 0100 | 1.0679ns | 0 | Deselect | 0 | |
| T | -6 | 0100 | 1.0679ns | 0 | Deselect | 0 | |
| | -5 | 0088 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=88 | 0 | |
| | -4 | 0110 | 1.0679ns | 0 | Deselect | 0 | |
| | -3 | 0110 | 1.0679ns | 0 | Deselect | 0 | |
| | -2 | 0110 | 1.0679ns | 0 | Deselect | 0 | |
| | -1 | 0090 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=90 | 0 | |
| T | 0 | 0000 | 1.0679ns | 5 | PRE Rank 0 Bank=5 | 1 | V15 |
| | 1 | 0000 | 1.0679ns | 5 | Deselect | 0 | |
| | 2 | 0000 | 1.0679ns | 5 | Deselect | 0 | |
| | 3 | 0098 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=98 | 0 | |
| | 4 | 0118 | 1.0679ns | 0 | Deselect | 0 | |
| | 5 | 0118 | 1.0679ns | 0 | Deselect | 0 | |
| | 6 | 0118 | 1.0679ns | 0 | Deselect | 0 | |
| | 7 | 00C0 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=C0 | 0 | |
| | 8 | 0120 | 1.0679ns | 0 | Deselect | 0 | |
| | 9 | 3F6E | 1.0679ns | 5 | ACT Rank 0 Bank=5 Addr=3F6E | 0 | |
| | 10 | 3F6E | 1.0679ns | 5 | Deselect | 0 | |
| | 11 | 00D0 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=D0 | 0 | |
| | 12 | 0128 | 1.0679ns | 0 | Deselect | 0 | |
| | 13 | 0128 | 1.0679ns | 0 | Deselect | 0 | |
| | 14 | 0128 | 1.0679ns | 0 | Deselect | 0 | |
| | 15 | 00C8 | 1.0679ns | 0 | RD Rank 1 Bank=0 Row=A27 Column=C8 | 0 | |
| | 16 | 0130 | 1.0679ns | 0 | Deselect | 0 | |

# How critical is this failure?

- A Precharge command closes the bank
- The DRAM is not expecting the Precharge command and may depend on that time to complete the Write
- Thousands of times per minute over months and years of operation may lead to data corruption

# Activate command too soon after a Calibration command

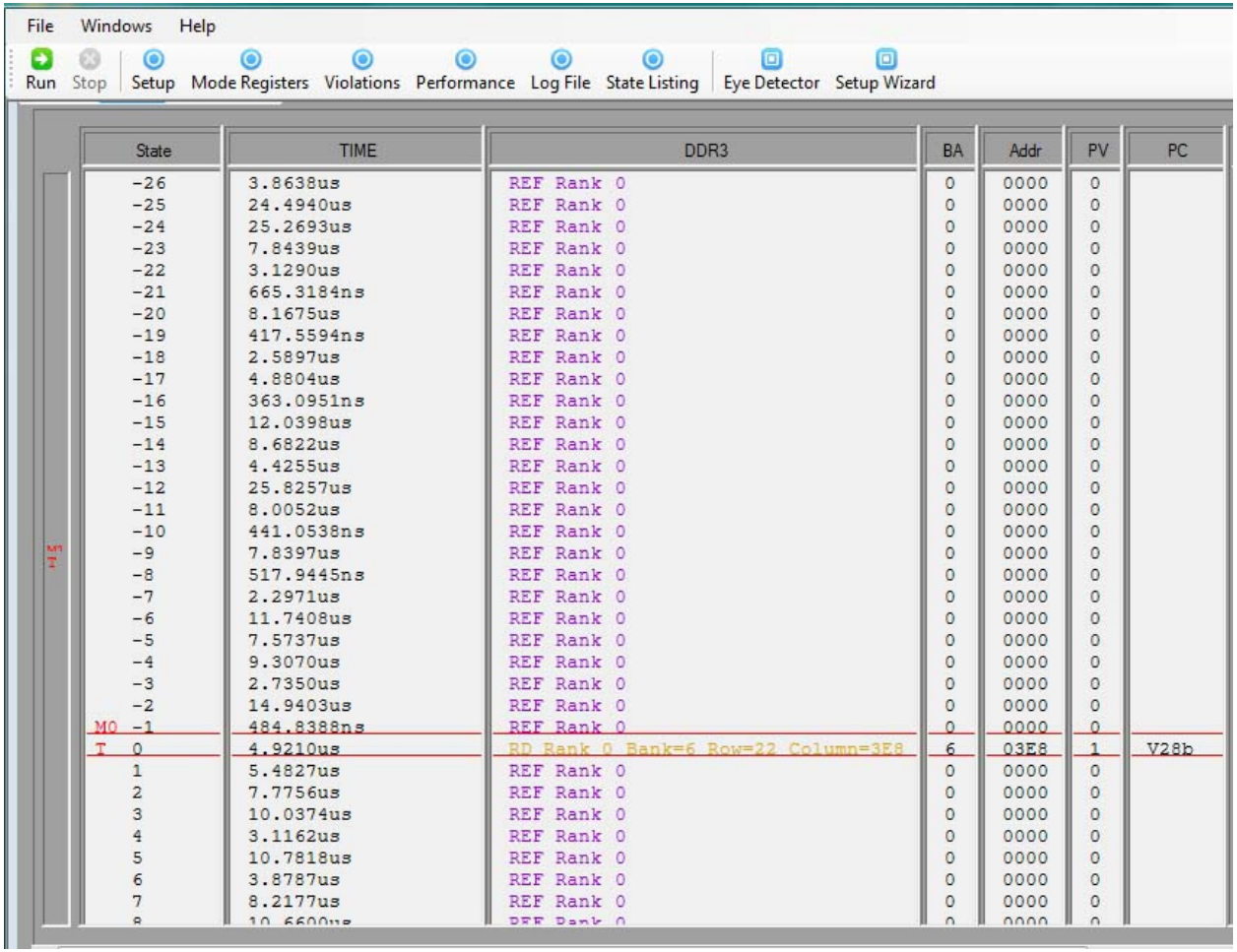



| | State | TIME | DDR3 | BA | Addr | PV | PC |
|---|---|---|---|---|---|---|---|
| | -2 | --- | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | -1 | 15.9290ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| T | 0 | 72.6191ns | ACT Rank 1 Bank=7 Addr=1A5F | 7 | 1A5F | 1 | V29a |
| | 1 | 6.4076ns | ACT Rank 1 Bank=2 Addr=1A6D | 2 | 1A6D | 1 | V29a |
| | 2 | 111.4840ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 3 | 72.6191ns | ACT Rank 0 Bank=1 Addr=5E0 | 1 | 05E0 | 1 | V29a |
| M0 | 4 | 15.9285ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| M1 | 5 | 72.6191ns | ACT Rank 1 Bank=1 Addr=374 | 1 | 0374 | 1 | V29a |
| | 6 | 111.4837ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 7 | 71.5512ns | ACT Rank 0 Bank=1 Addr=1204 | 1 | 1204 | 1 | V29a |
| | 8 | 6.4076ns | ACT Rank 0 Bank=5 Addr=11CC | 5 | 11CC | 1 | V29a |
| | 9 | 15.9286ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| | 10 | 72.6191ns | ACT Rank 1 Bank=2 Addr=155C | 2 | 155C | 1 | V29a |
| | 11 | 111.4841ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 12 | 72.6191ns | ACT Rank 0 Bank=0 Addr=29A5 | 0 | 29A5 | 1 | V29a |
| | 13 | 6.4076ns | ACT Rank 0 Bank=7 Addr=296E | 7 | 296E | 1 | V29a |
| | 14 | 15.9288ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| | 15 | 72.6191ns | ACT Rank 1 Bank=0 Addr=2D19 | 0 | 2D19 | 1 | V29a |
| | 16 | 6.4076ns | ACT Rank 1 Bank=6 Addr=2C60 | 6 | 2C60 | 1 | V29a |
| | 17 | 111.4840ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 18 | 71.5512ns | ACT Rank 0 Bank=2 Addr=3D95 | 2 | 3D95 | 1 | V29a |
| | 19 | 6.4076ns | ACT Rank 0 Bank=7 Addr=3DCC | 7 | 3DCC | 1 | V29a |
| | 20 | 15.9282ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| | 21 | 72.6191ns | ACT Rank 1 Bank=3 Addr=3B44 | 3 | 3B44 | 1 | V29a |
| | 22 | 6.4076ns | ACT Rank 1 Bank=7 Addr=3B3C | 7 | 3B3C | 1 | V29a |
| | 23 | 111.4843ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 24 | 72.6191ns | ACT Rank 0 Bank=3 Addr=2609 | 3 | 2609 | 1 | V29a |
| | 25 | 6.4076ns | ACT Rank 0 Bank=2 Addr=2678 | 2 | 2678 | 1 | V29a |
| | 26 | 15.9285ms | ZQCS Rank 1 | 0 | 0000 | 0 | |
| | 27 | 111.4840ms | ZQCS Rank 0 | 0 | 0000 | 0 | |
| | 28 | 71.5512ns | ACT Rank 0 Bank=6 Addr=E7C | 6 | 0E7C | 1 | V29a |

# How critical is this failure?

- Calibration commands – Purpose of calibrations is to account for voltage and temperature variations
- "No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibrations of output driver and on-die termination values"
- If the DRAM does not expect the Activate Command it may be missed and the row not opened

# A study of tREFI for the system under test




| State | TIME | DDR3 | BA | Addr | PV | PC |
|---|---|---|---|---|---|---|
| -26 | 3.8638us | REF Rank 0 | 0 | 0000 | 0 | |
| -25 | 24.4940us | REF Rank 0 | 0 | 0000 | 0 | |
| -24 | 25.2693us | REF Rank 0 | 0 | 0000 | 0 | |
| -23 | 7.8439us | REF Rank 0 | 0 | 0000 | 0 | |
| -22 | 3.1290us | REF Rank 0 | 0 | 0000 | 0 | |
| -21 | 665.3184ns | REF Rank 0 | 0 | 0000 | 0 | |
| -20 | 8.1675us | REF Rank 0 | 0 | 0000 | 0 | |
| -19 | 417.5594ns | REF Rank 0 | 0 | 0000 | 0 | |
| -18 | 2.5897us | REF Rank 0 | 0 | 0000 | 0 | |
| -17 | 4.8804us | REF Rank 0 | 0 | 0000 | 0 | |
| -16 | 363.0951ns | REF Rank 0 | 0 | 0000 | 0 | |
| -15 | 12.0398us | REF Rank 0 | 0 | 0000 | 0 | |
| -14 | 8.6822us | REF Rank 0 | 0 | 0000 | 0 | |
| -13 | 4.4255us | REF Rank 0 | 0 | 0000 | 0 | |
| -12 | 25.8257us | REF Rank 0 | 0 | 0000 | 0 | |
| -11 | 8.0052us | REF Rank 0 | 0 | 0000 | 0 | |
| -10 | 441.0538ns | REF Rank 0 | 0 | 0000 | 0 | |
| -9 | 7.8397us | REF Rank 0 | 0 | 0000 | 0 | |
| -8 | 517.9445ns | REF Rank 0 | 0 | 0000 | 0 | |
| -7 | 2.2971us | REF Rank 0 | 0 | 0000 | 0 | |
| -6 | 11.7408us | REF Rank 0 | 0 | 0000 | 0 | |
| -5 | 7.5737us | REF Rank 0 | 0 | 0000 | 0 | |
| -4 | 9.3070us | REF Rank 0 | 0 | 0000 | 0 | |
| -3 | 2.7350us | REF Rank 0 | 0 | 0000 | 0 | |
| -2 | 14.9403us | REF Rank 0 | 0 | 0000 | 0 | |
| M0 -1 | 484.8388ns | REF Rank 0 | 0 | 0000 | 0 | |
| T 0 | 4.9210us | RD Rank 0 Bank=6 Row=22 Column=3E8 | 6 | 03E8 | 1 | V28b |
| 1 | 5.4827us | REF Rank 0 | 0 | 0000 | 0 | |
| 2 | 7.7756us | REF Rank 0 | 0 | 0000 | 0 | |
| 3 | 10.0374us | REF Rank 0 | 0 | 0000 | 0 | |
| 4 | 3.1162us | REF Rank 0 | 0 | 0000 | 0 | |
| 5 | 10.7818us | REF Rank 0 | 0 | 0000 | 0 | |
| 6 | 3.8787us | REF Rank 0 | 0 | 0000 | 0 | |
| 7 | 8.2177us | REF Rank 0 | 0 | 0000 | 0 | |
| 8 | 10.6600us | REF Rank 0 | 0 | 0000 | 0 | |

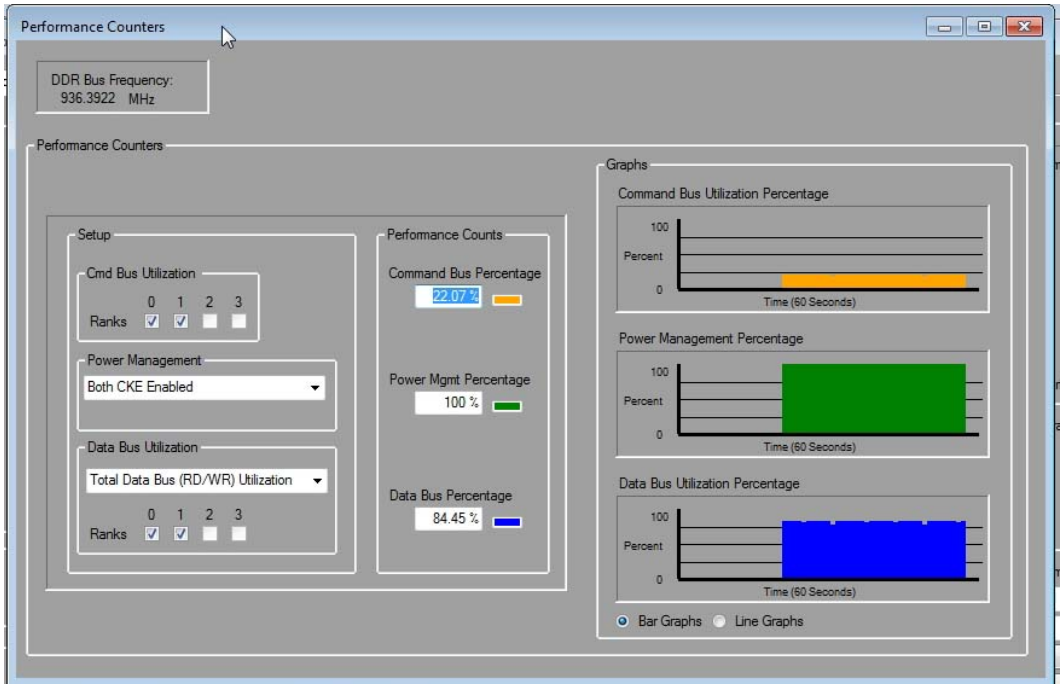
# Refreshes

- Purpose is to maintain the integrity of the stored data
- Refresh too much:  Waste power and bandwidth
- Refresh too little: Risk losing the data

# Performance Metrics

## *Real time measurement gives insight*

- Is power management as expected?
- Is Command bus and data bus utilization as expected?



# Summary

- Real Time Protocol Compliance Analysis of this type is now possible
- Designers can now make systems more reliable and gain a better understanding of compliance and performance metrics
- As memory technology becomes more critical to our society this insight will help us write better specifications and provide better products

# FuturePlus Systems Corporation

- Represented in China by CECEC

***www.cecec.com.cn***

- Represented in Shenzhen by HaoLun

***www.haoluntech.com***