Description of DDR4 Bus Violation Parameters for the FS2800 DDR Detective®

Applicability of check: Any = any occurrence, SR = Same Rank, SB = Same Bank DR = Same DIMM Different Rank DD = Different DIMM SBG = Same Bank Group DBG = Different Bank Group

Chk #	Violation Hardware Specification	App 1.	Parameters	PM Equation for DDR4 mode	Ex. 3.	Qty 5.
1	RD to RD < tCCD_L_R_cc *Similar to v26 in FS2400*	SBG	tCCD_L_R_cc 4 b ENABLE 1 b	tCCD_L_R_cc = tCCD_Lmin	5	16
2	RD to WR <tSR_RTW_cc *Similar to v15 in FS2400* Pulls in at BC4 OTF note 8.	SR	tSR_RTW_cc 5 b ENABLE 1 b	tSR_RTW_cc = READ to WRITE Command Delay = CL - CWL + 4 +2 Fixed8 or OTF = CL - CWL + 2 +2 Fixed4 note 8.	5	16
3	WR to WR < tCCD_L_W_cc *Similar to v6 in FS2400*	SBG	tCCD_L_W_cc 4 b ENABLE 1 b	tCCD_L_W_cc = tCCD_Lmin	5	16
4	RD to RD < tCCD_S_R_cc *Similar to v26 in FS2400*	DBG	tCCD_S_R_cc 4 b ENABLE 1 b	tCCD_S_R_cc = tCCD_Smin	4	4
5	WR to WR < tCCD_S_W_cc *Similar to v6 in FS2400*	DBG	tCCD_S_W_cc 4 b ENABLE 1 b	tCCD_S_W_cc = tCCD_Smin	4	4
6	Min ACT to ACT < tRRD_L_cc *Similar to v11 in FS2400*	SBG	tRRD_L_cc 4 b ENABLE 1 b	tRRD_L_cc = RU(tRRD_L{ns}/tCK{nS}) *Table 101, based on speed and Page size*	5	16
7	Min ACT to ACT < tRRD_S_cc *Similar to v11 in FS2400*	DBG	tRRD_S_cc 4 b ENABLE 1 b	tRRD_S_cc = RU(tRRD_S{ns}/tCK{nS}) *Table 101, based on speed and Page size*	4	4
8	5 ACT < tFAWmin < tFAW_cc *v40 in FS2400*	SR	tFAW_cc.....6 b ENABLE 1 b	tFAW_cc = RU(tFAW{ns}/tCK{ns}) *refer to Table 101, value based on speed and Page size (1/2, 1, 2K)*	20	4
9	WRITE to READ < tWTR_L_cc Is not pulled in by BC4 OTF.	SBG	tWTR_L_cc 6 b ENABLE 1 b	tWTR_L_cc =CWL+2+RU(tWTR_L{nS}/tCK{nS}) Fixed4 =CWL+4+RU(tWTR_L{nS}/tCK{nS}) Fixed8/OTF =CWL+5+RU(tWTR_L{nS}/tCK{nS}) CRC no DM =CWL+5+RU(tWTR_L_CRC_DM{nS}/tCK{nS}) CRC & DM are enabled	6 9 37	16

All values in nCK (number of clock cycles), unless marked with {ns}
Examples based on DDR4-1600 (tCK=1.25nS) and DDR4-2400 (tCK= 0.83nS)
OTF burst length is supported.
Not supported: 2tCK Write, Read Preamble, Gear Down Mode, PDA Mode, OTF Refresh rate
Assume: all ranks have identical devices and latencies.
Assume: CRC and DM enablement is not dynamic. OTF vs Fixed burst length mode is not dynamic.
Assume Fine Granularity Refresh 1X, 2X, 4X, OTF settings are not changed dynamically
Note: WL = CWL + AL + PL RL = CL + AL + PL (PL applies when CA parity latency mode enabled)
Max: 46 18 23 5 52 24 23 5
Note: Parameters in this chart (XXX_cc) are the values of latency tested between the stated events and may be defined differently than the similar-named JEDEC parameters.
JEDEC parameters are inputs to the PM equations and are defined in JESD79-4 (Table 101 mostly).
Assume: DDR4 “any command” or “valid command” includes the NOP command

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for DDR4 mode	Ex.	Qty
10	WRITE to READ < tWTR_S_cc Is not pulled in by BC4 OTF.	DBG	tWTR_S_cc 6 b ENABLE 1 b	tWTR_S_cc =CWL+2+RU(tWTR_S{nS}/tCK{nS}) Fixed4 =CWL+4+RU(tWTR_S{nS}/tCK{nS}) Fixed8/OTF =CWL+5+RU(tWTR_S{nS}/tCK{nS}) CRC no DM =CWL+5+RU(tWTR_S_CRC_DM{nS}/tCK{nS}) both CRC & DM are enabled	2	4
11	READ to PRE < tRTP_cc READ to PREA < tRTP_cc *v5 in FS2400*	SB SR	tRTP_cc 7 b ENABLE 1 b	tRTP_cc = RU(tRTP/tCK{ns}) + AL	6	64
12	WR to PRE< tWR_cc WR to PREA *Similar to v16 in FS2400* Is not pulled in by BC4 OTF.	SB SR	tWR_cc 7 b ENABLE 1 b	tWR_cc =WL+2+RU(tWR{nS}/tCK{nS}) Fixed4 =WL+4+RU(tWR{nS}/tCK{nS}) Fixed8/OTF =WL+5+RU(tWR_CRC_DM{nS}/tCK{nS}) both CRC & DM are enabled	12	64
13	DLL Reset (MR0 b8) to any command or CKE low < tDLLK_cc *v43 in FS2400*	SR	tDLLK_cc 10b ENABLE 1 b ODTEN* 1 b * not used	tDLLK_cc = tDLLK	597	4
14	MRS to MRS < tMRD_cc *v1 in FS2400*	SR	tMRD_cc 4 b ENABLE 1 b	tMRD_cc = tMRD	8	4
15	MRS to other Command or ODT high < tMOD_cc *v2 in FS2400*	SR	tMOD_cc 5 b ENABLE 1 b ODTEN 1 b	tMOD_cc = RU(tMOD{nS}/tCK{nS})	24	4
16	CA Bus (excluding CKE, ODT, and CS) and PAR_IN bit have an odd number of 1s (parity fail)	SR	reserved 4 b ENABLE 1 b	enable this test only in parity mode, ie when MR5 A2:0 is non-zero	NA	4
17	1st ZQCL after Reset low to High to any Command, ODT high, CKE Low < tZQinit_cc	SR	tZQinit_cc 11 b ENABLE 1 b ODTEN 1 b	tZQinit_cc = tZQinit	1k	4
18	All but the 1st ZQCL after Reset low to High to any Command, ODT high, CKE Low < tZQoper_cc *v38 in FS2400*	SR	tZQoper_cc 10 b ENABLE 1 b ODTEN 1 b	tZQoper_cc = tZQoper	512	4
19	Time from ZQCS to any Command, ODT high, CKE Low < tZQCS_cc *v37 in FS2400*	SR	tZQCS_cc 8 b ENABLE 1 b ODTEN 1 b	tZQCS_cc = tZQCS	128	4
20	Reset Low to High, then CKE Low to High to any Command or ODT High < tXPR_cc	SR	tXPR_cc 10 b ENABLE 1 b ODTEN 1 b	tXPR_cc = RU(tXPR{nS}/tck{nS})	288 433	4

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for DDR4 mode	Ex.	Qty
21	SRX to ACT, PRE, PREA, REF, SRE, PDE, WRITE, READ, or MRS < tXS_cc *v8 in FS2400* note 9.	SR	tXS_cc 10 b ENABLE 1 b	tXS_cc = RU(tXS{nS}/tCK{nS}) = RU((tRFCmin+10ns)/tCK{ns})	288 602	4
22	SRX to non-Deselect (ie any Command) < tXS_ABORT_cc	SR	tXS_ABORT_cc 9 b ENABLE 1 b	tXS_ABORT_cc = RU(tXS_ABORT{nS}/tCK{nS}) = RU((tRFC4+10ns)/tCK{ns}) Disable this check if MR4A9 is not set	136	4
23	SRX to ZQCL, ZQCS < tXS_FAST_cc note 9.	SR	tXS_FAST_cc 9 b ENABLE 1 b	tXS_FAST_cc = RU(tXS_FAST{nS}/tCK{nS}) = RU(tRFC4+10ns)/tCK{ns}	136	4
24	SRX to READ or CKE Low or ODT Hi < tXSDLL_cc *v10 in FS2400*	SR	tXSDLL_cc 10 b ENABLE 1 b ODTEN 1 b	tXSDLL_cc = tXSDLL = TBD ODT portion may be disabled in asynchronous mode (DLL-off mode)	597	4
25	SRE to SRX < tCKESR_cc (self-refresh, CKE low time) *v9 in FS2400*	SR	tCKESR_cc 4 b ENABLE 1 b	tCKESR_cc = tCKESR	5	4
26	PDX to non-Deselect (ie any Command) or ODT Hi < tXP_cc *v50 in FS2400* note 10.	SR	tXP_CC 4 b ENABLE 1 b	tXP_cc = RU(tXP{nS}/tCK{nS}) Disable this check in DLL-off mode	5	4
27	CKE min pulse width < tCKEmin_cc Test hi time and low time *v46 in FS2400*	SR	tCKEmin_cc 4 b ENABLE 1 b	tCKEmin_cc = RU(tCKEmin{nS}/tCK{ns})	4	4
28	PDE to PDX < tPDmin_cc (min Powerdown time) *v48 in FS2400* note 6.	SR	tPDmin_cc 4 b ENABLE 1 b	tPDmin_cc = RU(tPDmin{nS}/tCK{ns})	4	4
29	PDE to PDX > tPDmax_cc (max Powerdown time) *v49 in FS2400* note 4. note 6. note 13.	SR	tPDmax_cc 17 b ENABLE 1 b	tPDmax_cc = RU (tPDmax{nS}/tCK{nS}) = RU (9*tREFI{nS}/tCK{ns})	56160 84576	4
30	ACT to PDE < tACTDPEN_cc	SR	tACTPDEN_cc 4 b ENABLE 1 b	tACTPDEN_cc = tACTPDEN Disable this check when = 1	2	4
31	PRE or PREA to PDE < tPRPDEN_cc	SR	tPRPDEN_cc 4 b ENABLE 1 b ODTEN 1 b	tPRPDEN_cc = tPRPDEN Disable this check when = 1	2	4
32	RD or RDA to PDE < tRDPDEN_cc	SR	tRDPDEN_cc 7 b ENABLE 1 b	tRDPDEN_cc = tRDPDEN = CL+AL+PL+5	16 57	4
33	WR to PDE < tWRPDEN_cc Is not pulled in by BC4 OTF.	SR	tWRPDEN_cc 7 b ENABLE 1 b	tWRPDEN _cc = tWRPDEN = WL+4+ RU(tWR{nS}/tCK{ns}) Disable this check when in Fixed4 mode	27	4
34	WRA to PDE < tWRAPDEN _cc Is not pulled in by BC4 OTF.	SR	tWRAPDEN_cc 7 b ENABLE 1 b	tWRAPDEN _cc = tWRAPDEN = WL+5+ RU(tWR{nS}/tCK{ns}) Disable this check when in Fixed4 mode	31	4

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for DDR4 mode	Ex.	Qty
35	WR to PDE < tWRPBC4DEN_cc Is not pulled in by BC4 OTF.	SR	tWRPBC4DEN_cc 7 b ENABLE 1 b	tWRPDEN _cc = tWRPDEN = WL+2+ RU(tWR{nS}/tCK{ns}) Enable this check when in Fixed4 mode	25	4
36	WRA to PDE < tWRAPBC4DEN_cc Is not pulled in by BC4 OTF.	SR	tWRAPBC4DEN_cc 7 b ENABLE 1 b	tWRAPDEN _cc = tWRAPDEN = WL+3+ RU(tWR{nS}/tCK{ns}) Enable this check when in Fixed4 mode	23	4
37	REF to PDE < tREFPDEN_cc	SR	tREFPDEN_cc 2 b ENABLE 1 b	tREFPDEN_cc = tREFPDEN Disable when = 1	1	4
38	MRS to PDE < tMRSPDEN_cc	SR	tMRSPDEN_cc 5 b ENABLE 1 b	tMRSPDEN_cc = RU (tMRSPDEN{ns}/tck{ns})	24	4
39	PRE to ACT < tRP_cc PREA to ACT < tRP_cc PRE or PREA to ZQCS, ZQCL, MRS, REF, SRE < tRP_cc *v4 in FS2400* note 11.	SB SR SR	tRP_cc 5 b ENABLE 1 b	tRP_cc = RU(tRP{nS}/tCK{ns})	11 18	64
40	ACT to PRE < tRASmin_cc ACT to PREA < tRASmin_cc *v13 in FS2400*	SB SR	tRASmin_cc 6 b ENABLE 1 b	tRASmin_cc = RU(tRASmin{nS}/tCK{ns})	28 42	64
41	ACT to PRE or AutoPrech> tRASmax_cc ACT to PREA >tRASmax_cc *v14 in FS2400* note 13.	SB SR	tRASmax_cc 17 b ENABLE 1 b	tRASmax_cc = RU(tRASmax{nS}/tCK{nS}) = RU(9*tREF/tCK{ns})	56160	64
42	ACT to RD or WR < tRCD_cc *v3 in FS2400*	SB	tRCD_cc 6 b ENABLE 1 b	tRCD_cc = RU(tRCD{nS}/tCK{ns}) - AL Disable check when tRCD_cc =1 or <1	11 18	64
43	ACT to ACT or REF < tRC_cc	SB	tRC_cc 7 b ENABLE 1 b	tRC_cc = RU(tRC{nS}/tCK{ns})	39	64
44	REF to non-Des (any Command) < tRFC_cc *v7 in FS2400*	SR	tRFC_cc 10 b ENABLE 1 b	tRFC_cc = RU(tRFC1{nS}/tCK{ns}) x1 REF mode = RU(tRFC2{nS}/tCK{ns}) x2 REF mode = RU(tRFC4{nS}/tCK{ns}) x4 REF mode	128	4
45	REF to REF avg Interval > tREFIavg_cc (with no intervening SR) Averaged over 128 REFRESH commands.	SR	tREFIavg_cc 15 b ENABLE 1 b	tREFIavg_cc = = RU(tREFI1{ns}/tCK{ns}) x1 REF mode = RU(tREFI2{ns}/tCK{ns}) x2 REF mode = RU(tREFI4{ns}/tCK{ns}) x4 REF mode tREFI numbers depend on temperature. Tables 23 and 100	6240 9398	4
46	REF to REF max Interval <tREFImax_cc (with no intervening SR) *v35 in FS2400* note 12. note 13.	SR	tREFImax_cc 17 b ENABLE 1 b	tREFImax_cc = = RU(9 * tREFI1{ns}/tCK{ns}) x1 REF = RU(17 * tREFI2{ns}/tCK{ns}) x2 REF = RU(33 * tREFI4{ns}/tCK{ns}) x4 REF tREFI numbers depend on temperature. Tables 23 and 100	56160	4
47	Read or Write to an Inactive Bank. (must see RESET# or PRE/PREA to know banks are inactive.) *v18 in FS2400*	SB	ENABLE 1 b			64
48	Refresh to an Active Bank (must see 1st Activate to know SB bank is active.) *v19 in FS2400*	SB	ENABLE 1 b			64

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for DDR4 mode	Ex.	Qty
49	Activate to an Active bank (Must see 1st Activate to know bank is active.) *v20 in FS2400*	SB	ENABLE 1 b			64
50	MRS with an Active Bank (Must see Activate to know bank is active.) *v21 in FS2400*	SR	ENABLE 1 b			4
51	Self Refresh Entry with an Active Bank *v22 in FS2400*	SR	ENABLE 1 b			4
52	ZQCS or ZQCL with an Active bank *v23 in FS2400*	SR	ENABLE 1 b			4
53	Read to Read < tDR_RTR_cc *v27 in FS2400* note 8. pulls in at BC4 OTF	DR	tDR_RTR_cc 4 b ENABLE 1 b	tDR_RTR_cc = 2 +1 Fixed4 = 4 +1 Fixed8 or OTF +1 is for Read preamble time note 8.	5	4
54	Read to Read < tDD_RTR_cc *v28 in FS2400* note 8. pulls in at BC4 OTF	DD	tDD_RTR_cc 4 b ENABLE 1 b	tDD_RTR_cc = 2 +1 Fixed4 = 4 +1 Fixed8 or OTF +1 is for Read preamble time note 8.	5	2
55	Read to Write < tDR_RTW_cc *v29 in FS2400* note 8. pulls in at BC4 OTF	DR	tDR_RTW_cc ...4 b ENABLE 1 b	tDR_RTW_cc = CL- CWL + 2 +1 Fixed4 = CL- CWL + 4 +1 Fixed8 or OTF +1 is for Write preamble time note 8.		4
56	Read to Write < tDD_RTW_cc *v30 in FS2400* note 8. pulls in at BC4 OTF	DD	tDD_RTW_cc 4 b ENABLE 1 b	tDD_RTW_cc = CL- CWL + 2 +1 Fixed4 = CL- CWL + 4 +1 Fixed8 or OTF +1 is for Write preamble time note 8.		2
57	Write to Read < tDR_WTR_cc *v31 in FS2400* note 8. pulls in at BC4 OTF	DR	tDR_WTR_cc 6 b ENABLE 1 b	tDR_WTR_cc = CWL- CL + 2 +1 Fixed4 = CWL- CL + 4 +1 Fixed8 or OTF = CWL- CL + 5 +1 CRC & DM mode +1 is for Read preamble time note 8.		4
58	Write to Read < tDD_WTR_cc *v32 in FS2400* note 8. pulls in at BC4 OTF	DD	tDD_WTR_cc 6 b ENABLE 1 b	tDD_WTR_cc = CWL- CL + 2 +1 Fixed4 = CWL- CL + 4 +1 Fixed8 or OTF = CWL- CL + 5 +1 CRC & DM mode +1 is for Read preamble time note 8.		2
59	Write to Write < tDR_WTW_cc *v33 in FS2400* note 8. pulls in at BC4 OTF	DR	tDR_WTW_cc... 4 b ENABLE 1 b	tDR_WTW_cc = 2 +1 Fixed4 = 4 +1 Fixed8 or OTF = 5 +1 CRC & DM +1 is for Write preamble time note 8.		4
60	Write to Write < tDD_WTW_cc *v34 in FS2400* note 8. pulls in at BC4 OTF	DD	tDD_WTW_cc 4 b ENABLE 1 b	tDD_WTW_cc = 2 +1 Fixed4 = 4 +1 Fixed8 or OTF = 5 +1 CRC & DM +1 is for Write preamble time note 8.		2

Chk #	Violation Hardware Specification	App	Parameters	PM Equation for DDR4 mode	Ex.	Qty
61	ODT hi to low time < ODTH4_cc	SR	tODTH4_cc 4 b ENABLE 1 b	tODTH4_cc = ODTH4 = 2 Fixed4 Mode Enable this check when in Fixed4 mode	4	4
62	ODT hi to low time < ODTH8_cc note 8. pulls in at BC4 OTF	SR	tODTH8_cc 4 b ENABLE 1 b	tODTH8_cc = ODTH8 = 4 Fixed8 or OTF = 5 CRC & DM enabled Disable this check when in Fixed4 mode note 8.	6	4
63	PDE or SRE followed by non-DES < tCPDED_cc	SR	tCPDED_cc 4 b ENABLE 1 b	tCPDED_cc = tCPDED =4	4	4
64	WRA to ACT < tDAL_cc WRA to ZQCS, ZQCL, MRS, REF, SRE < tDAL_cc (is not pulled in by OTF) *v39 in FS2400*	SB SR	tDAL_cc 7 b ENABLE 1 b	tDAL_cc = WL + 2 + RU(tWR{nS}/tCK[nS}) + RU(tRP{nS}/tCK{ns}) Fixed 4 = WL + 4 + RU(tWR{nS}/tCK[nS}) + RU(tRP{nS}/tCK{ns}) Fixed8/OTF	86	64
65	RDA to ACT < tRAP_cc RDA to ZQCS, ZQCL, MRS, REF, SRE < tRAP_cc (is not pulled in by OTF) *v39 in FS2400*	SB SR	tRAP_cc 7 b ENABLE 1 b	tRAP_cc = RU(tRTP/tCK{nS}) + RU(tRP/tCK{nS}) + AL Note: tRAP is not a JEDEC name	27 50	64

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