JEDEC®

Global Standards for the Microelectronics Industry

DDR Compliance Testing
Its time has come!

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Server Forum 2014

DDR Compliance Testing

- If not then why now?
  - Continued growth and reliance on DDR memory
  - Critical applications increasing
  - Errors don’t scale well
    - Large Data Centers replacing DIMMs every hour

Several Publications point to error rate much larger than expected

- DRAM Errors in the Wild: A Large-Scale Field Study *Sigmetrics 2009*
- Cosmic Rays Don't Strike Twice: Understanding the Nature of DRAM Errors and the Implications for System Design by Andy Hwang, Ioan Stefanovici and Bianca Schroeder)
- A Field Study of DRAM Errors 2012 by Sridharan, Liberty, RAS Architecture AMD
- Reliability, Serviceability and Availability: Intel XEON Processor E7 Family April 2014
- Characterizing Application Memory Error Vulnerability to Optimize Datacenter Cost via Hetrogeneous-Reliability Memory June 2014 Microsoft
- Avoiding server downtime from hardware errors in system memory with HP Memory Quarantine HP Technology Brief January 2012
- Flipping bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors by Yoongu Ki, et al Carnegie Mellon University and Intel Labs July 2014

Open Compute Project

- Ready Certification
- Compliant Certification
  - Will point at other standards…if they exist
- Certification labs
  - University of Texas San Antonio
  - ITRI (Taiwan)
- You can Join! www.OCP.com

National Institute of Standards and Technology

- Information Technology Laboratories
  - Cloud Computing Program

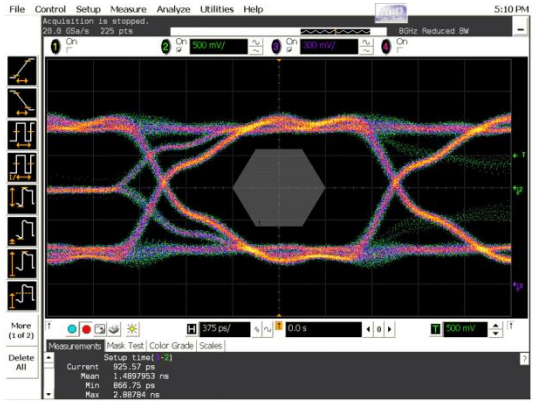
*"…It is **considered critical** that government and industry begin adoption of this technology in response to difficult economic constraints. …..Cloud computing is currently being used; however, security, interoperability, and portability are cited as major barriers to broader adoption….The long term goal is to provide thought leadership and guidance around the cloud computing paradigm to catalyze its use within industry and government. NIST aims to **shorten the adoption cycle**…. NIST aims **to foster cloud computing systems and practices** that support **interoperability, portability, and security requirements** that are appropriate and achievable for important usage scenarios."*

What would DDR4 Compliance Testing Look Like?

- DRAM specific
  - DIMM/SODIMM/LRDIMM
- Memory Controller specific
- The path between the two
- A Compliance Test Specification
  - T&M Vendors can produce MOI (Method of Implementation)
  - End users can then request this testing
    - Compliance Lab Testing

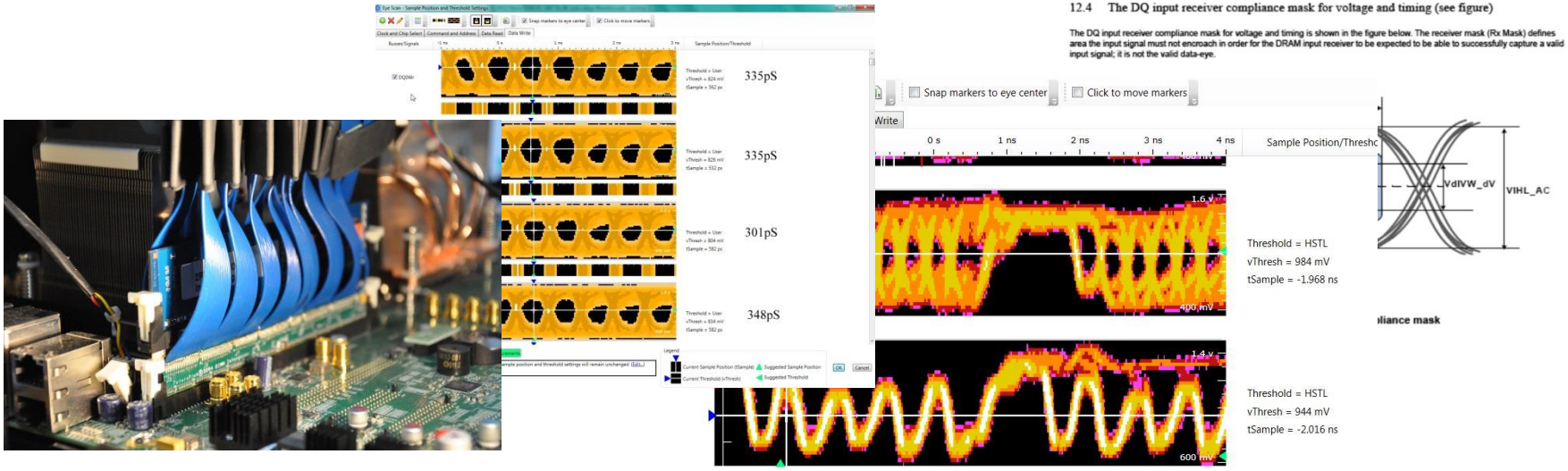
DDR4 Compliance Testing

- Memory Controller Specific
  - RX/TX eye specification
    - Bit Error Rate
  - Protocol Violations
  - Timing Violations
  - Performance Specifications



Memory Controller RX/TX

- Compliance Masks
- Measurement can be made with an interposer
  - Qualitative -> Quantitative

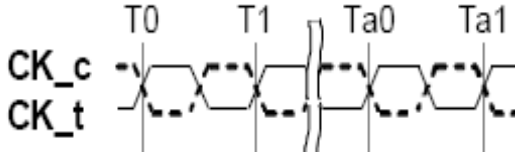


Memory Controller *Protocol Violations*

- The DDR4 JEDEC spec contains rules on event ordering
  - Examples
    - Do not ACTIVATE a bank that is already open
    - Do not PRECHARGE a bank that is already closed
    - Do not RD/WR a non open page

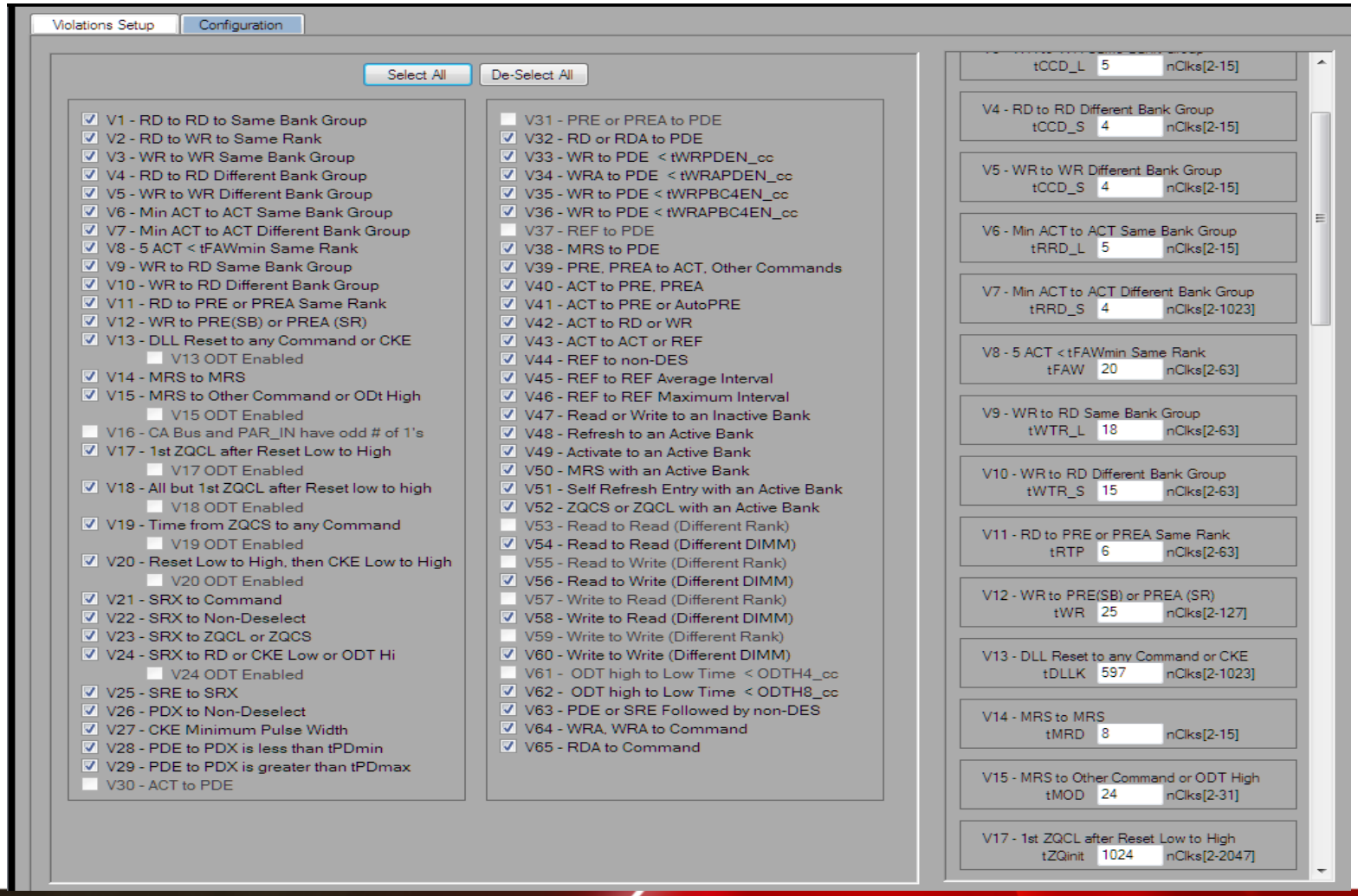
Memory Controller
Timing Violations

- Clock edge boundary

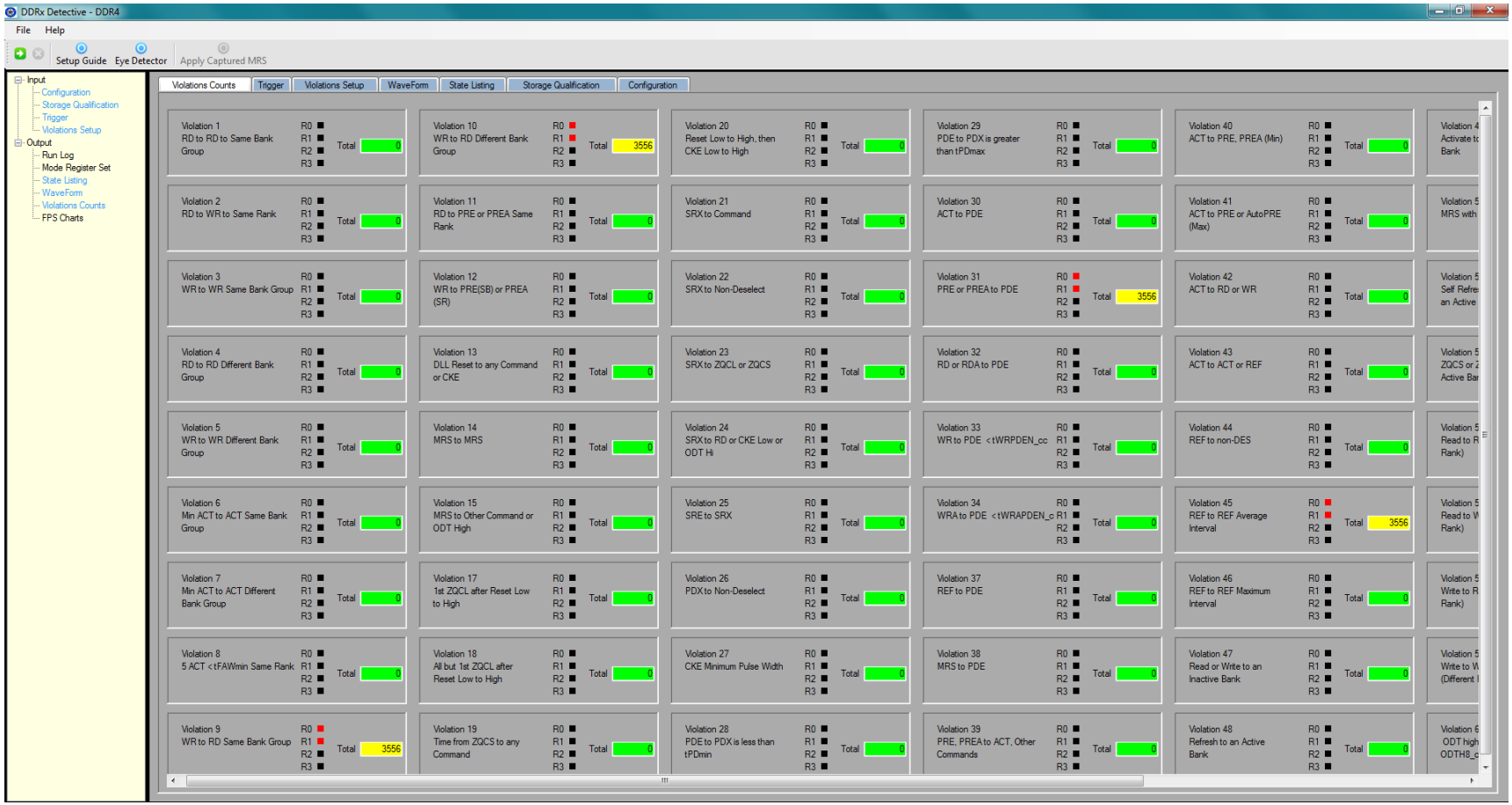


  - Things can not be too close together or too far apart
  - Examples
    - tREFI Average refresh interval
    - tRC ACT ot ACT or REF
    - tMOD MRS to PDE
    - tCCD_L RD to RD to Same Bank Group

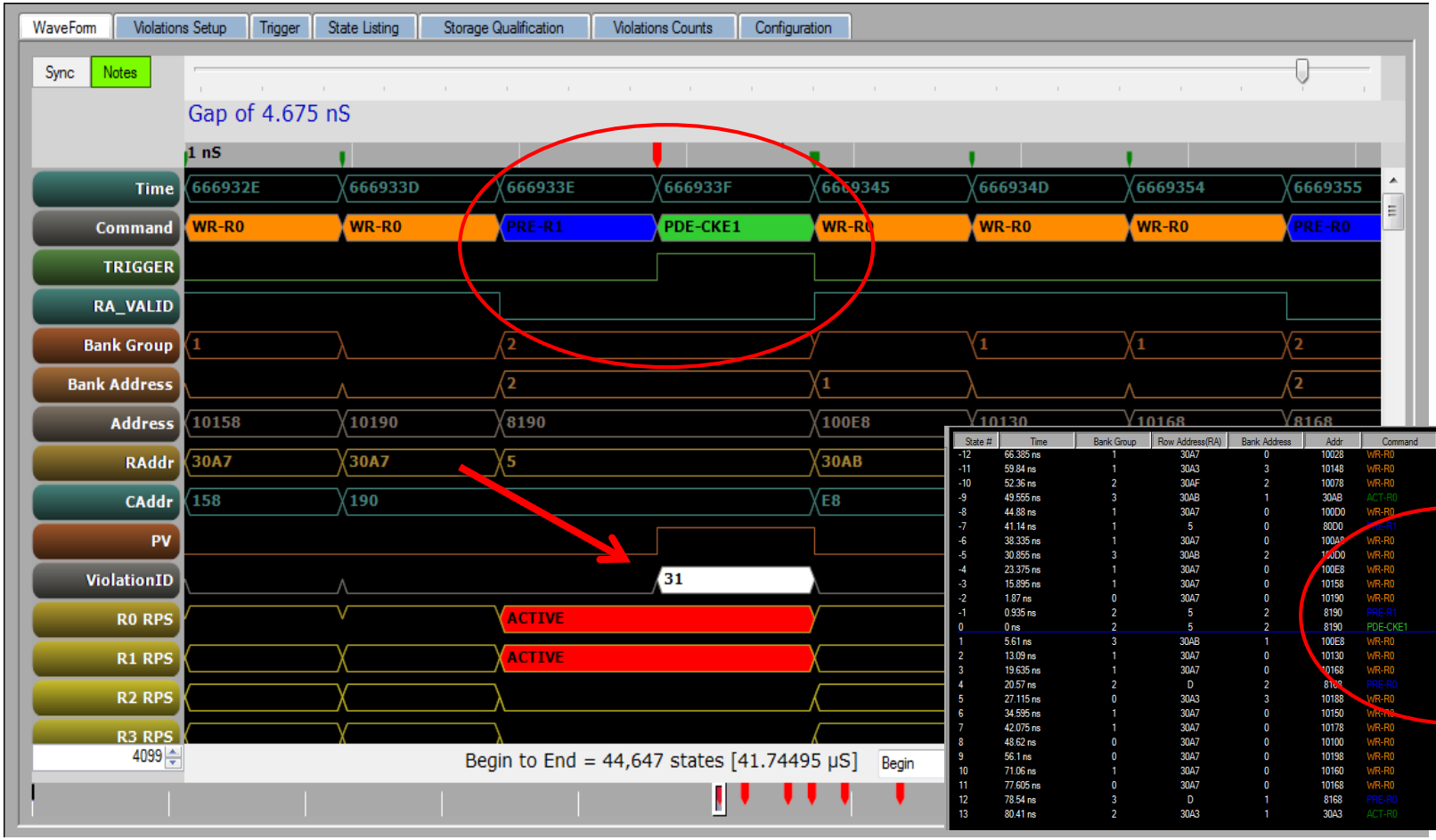
65 violations identified with over 1000+ simultaneous checks



Protocol and Timing Compliance ‘in the wild’



JEDEC Specification Violation

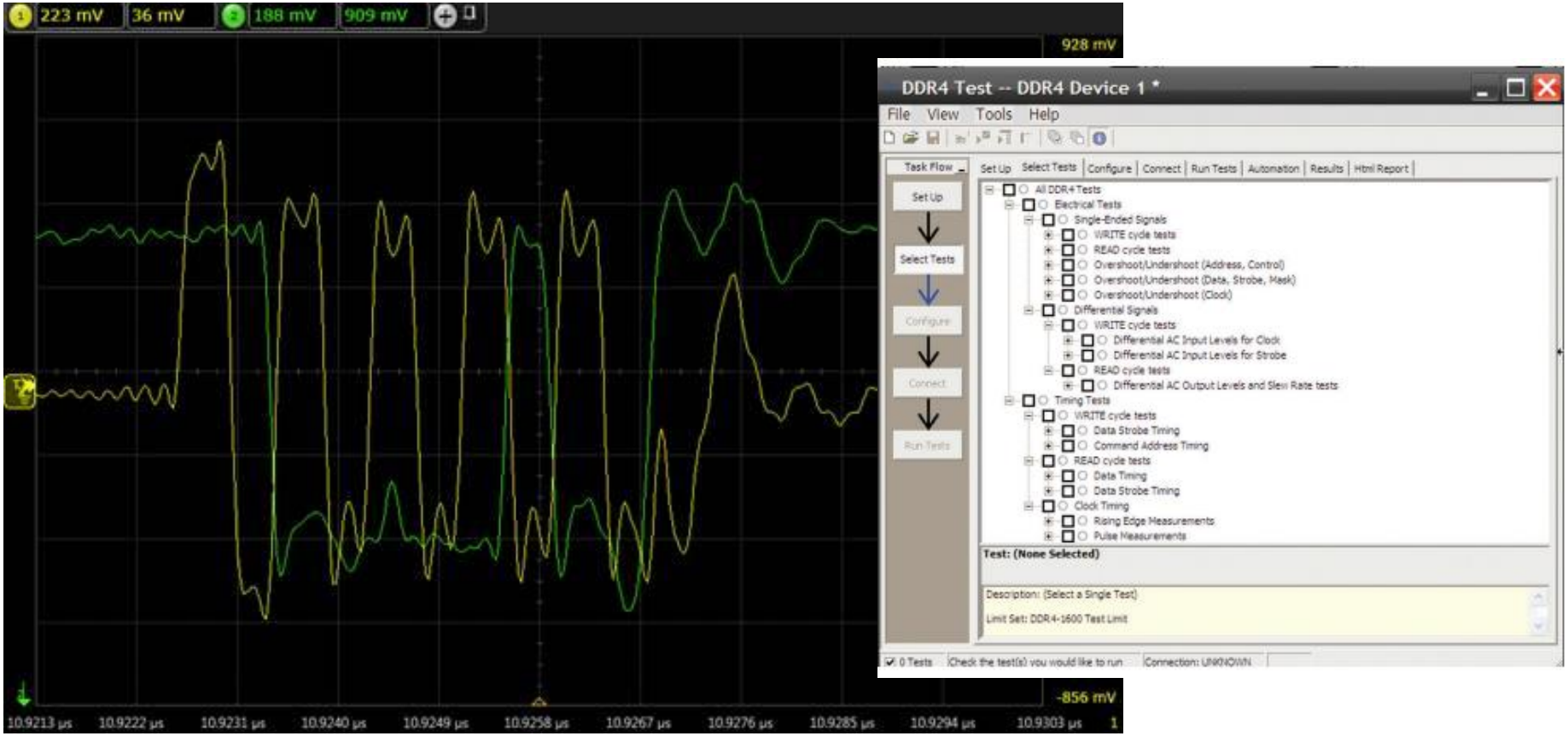


State #	Time	Bank Group	Row Address(RA)	Bank Address	Addr	Command	Violation(PV)	ViolationID
-12	66.385 ns	1	30A7	0	10028	WR-R0	0	
-11	59.84 ns	1	30A3	3	10148	WR-R0	0	
-10	52.36 ns	2	30AF	2	10078	WR-R0	0	
-9	49.555 ns	3	30AB	1	30AB	ACT-R0	0	
-8	44.88 ns	1	30A7	0	100D0	WR-R0	0	
-7	41.14 ns	1	5	0	80D0	PRE-R1	0	
-6	38.335 ns	1	30A7	0	100A8	WR-R0	0	
-5	30.855 ns	3	30AB	2	100D0	WR-R0	0	
-4	23.375 ns	1	30A7	0	100E8	WR-R0	0	
-3	15.895 ns	1	30A7	0	10158	WR-R0	0	
-2	1.87 ns	0	30A7	0	10190	WR-R0	0	
-1	0.935 ns	2	5	2	8190	PRE-R1	0	
0	0 ns	2	5	2	8190	PDE-CKE1	1	31
1	5.61 ns	3	30AB	1	100E8	WR-R0	0	
2	13.09 ns	1	30A7	0	10130	WR-R0	0	
3	19.635 ns	1	30A7	0	10168	WR-R0	0	
4	20.57 ns	2	D	2	8168	PRE-R0	0	
5	27.115 ns	0	30A3	3	10188	WR-R0	0	
6	34.595 ns	1	30A7	0	10150	WR-R0	0	
7	42.075 ns	1	30A7	0	10178	WR-R0	0	
8	48.62 ns	0	30A7	0	10100	WR-R0	0	
9	56.1 ns	0	30A7	0	10198	WR-R0	0	
10	71.06 ns	1	30A7	0	10160	WR-R0	0	
11	77.605 ns	0	30A7	0	10168	WR-R0	0	
12	78.54 ns	3	D	1	8168	PRE-R0	0	
13	80.41 ns	2	30A3	1	30A3	ACT-R0	0	

Memory Controller
Timing Violations

- Timing that occurs between clock edges
  - Setup/Hold
  - Eye Mask
  - Jitter

Several Scope Vendors have DDR4 Compliance Products



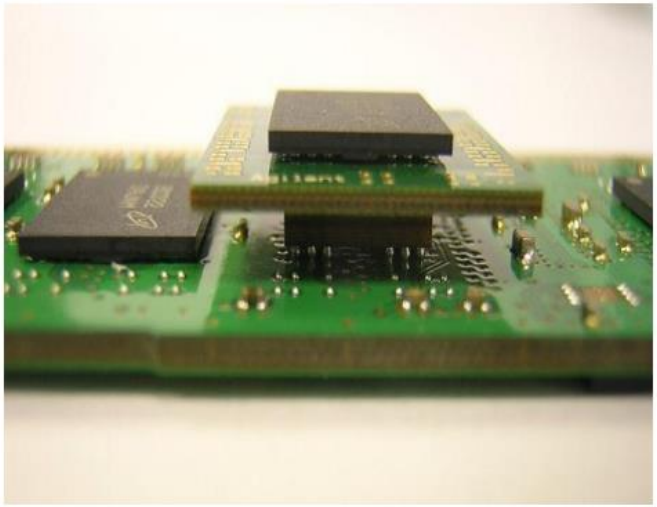
Performance Metrics

- BER testing at particular transfer rates
  - 1E-16
- Which power management features are implemented
  - Is the clock stopped in Self Refresh?
  - Is Max Power Down implemented?

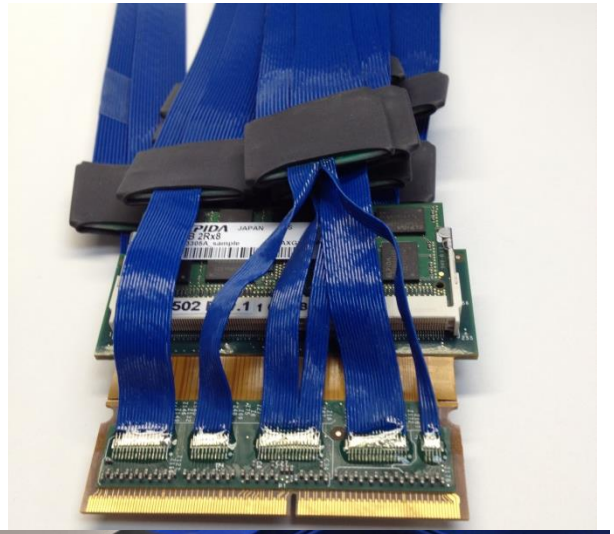
DDR4 Compliance Testing

- DRAM Specific
  - DIMM/SODIMM/LRDIMM
  - RX/TX eye specification
    - Bit Error Rate
  - Data Integrity
    - Row Hammer (Excessive Activates)
  - Functional/Timing Verification
  - Performance Verification

Making the Measurement



Photos Courtesy of Keysight Technologies

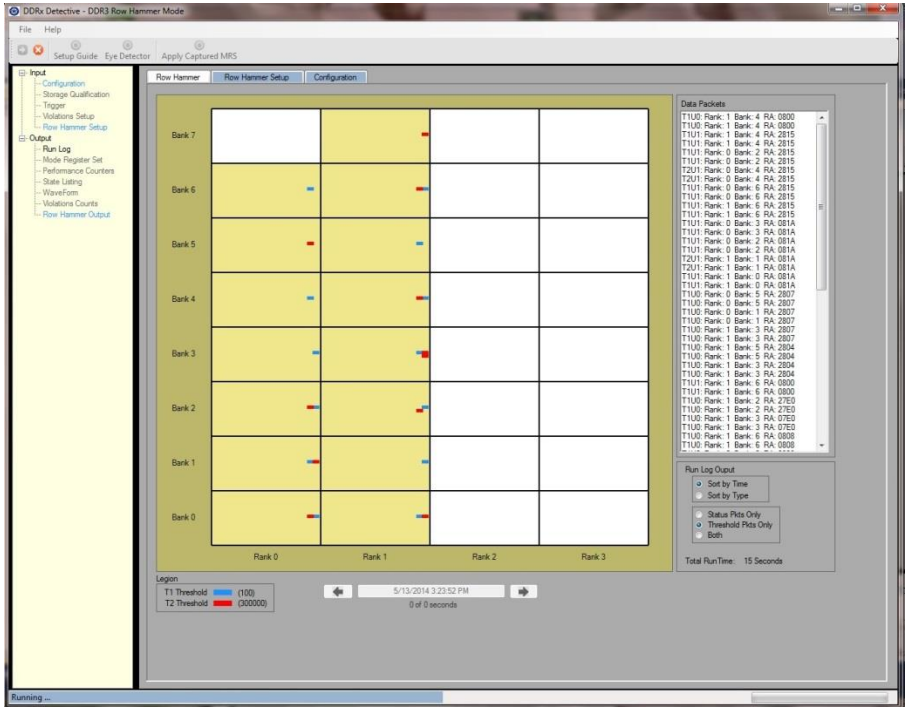


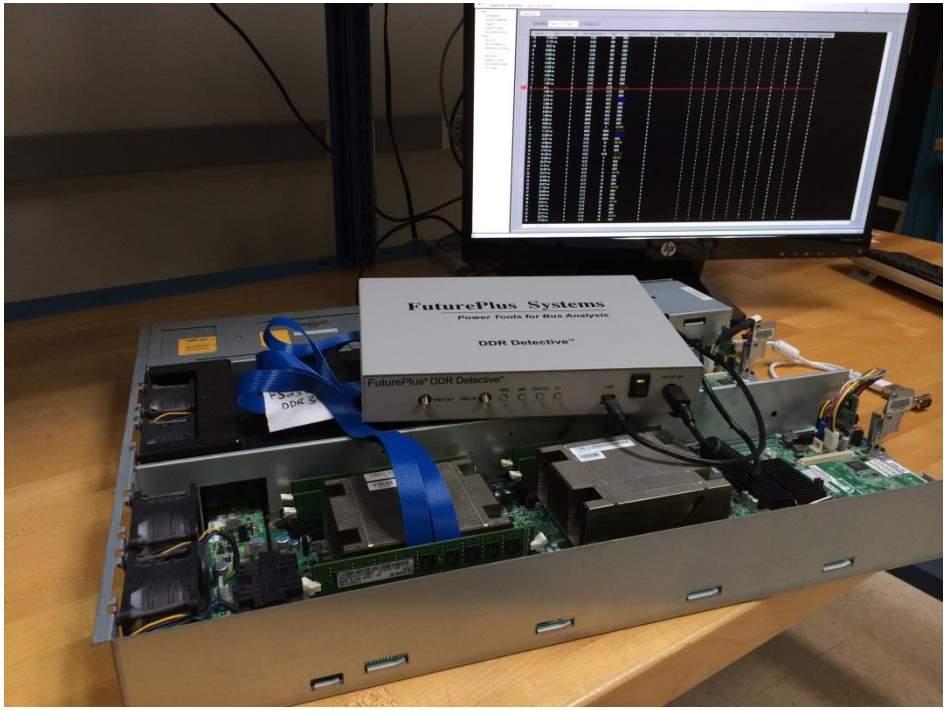
Photos Courtesy of FuturePlus Systems

Row Hammer: Excessive Activates

- Yes its real…..easy to reproduce with software memory tests
- CMU study is the most recent technical paper on the topic
- Tools now look for it
- Data Centers are seeing it

Row Hammer Detection





Row Hammer detection feature of the DDR Detective® lists the row address when the number of ACT commands exceeds a threshold within 64ms. Two programmable thresholds are available

Testing a Server for Row Hammer using the DDR Detective® with software from ThirdIO

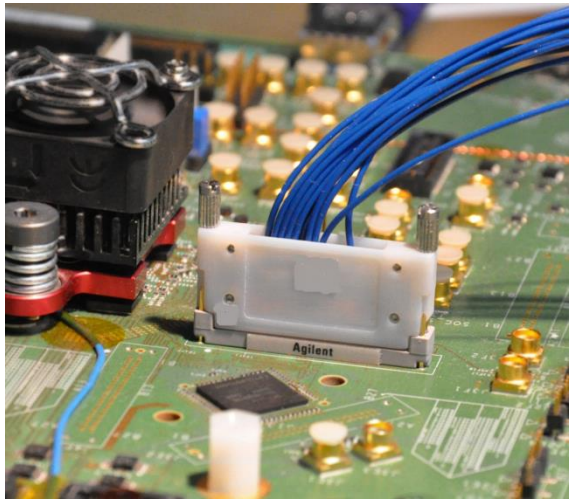
The electrical path between the DRAM and the Memory Controller

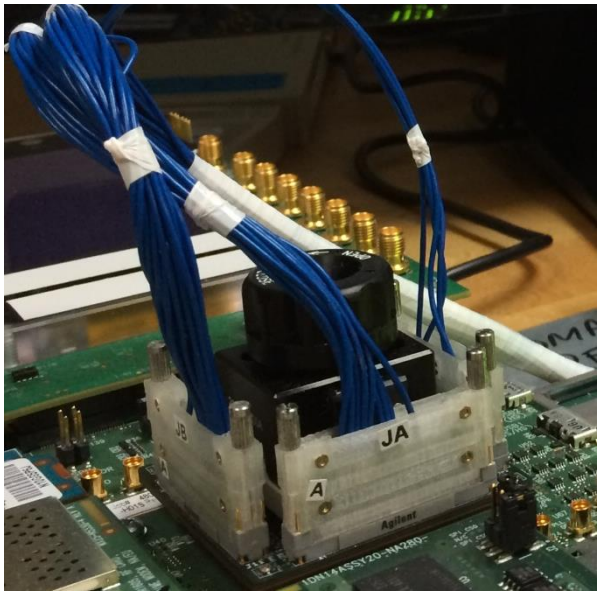
- End to End Measurements to verify channel integrity
- Require Slot/Channel loading configurations based on speed/eye size
- Memory channel layout/board files with simulation results?
  - Similar to what is done today with raw cards

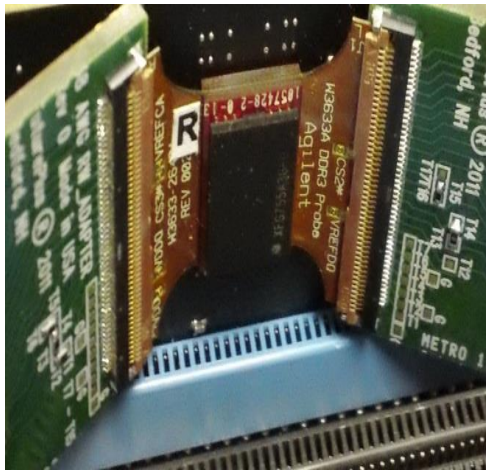
What about the LP DDR specifications?

- Many of the tests are applicable and can be reused
- Probing becomes more difficult but can be accomplished
- Measuring Power Management features becomes more critical

LPDDRx Compliance Test







Advantages to having a Compliance Test Spec

- It is going to help our industry
  - End users are asking for this!
- Helps eliminate ambiguities in the specification
  - Ex: tREFI=Average Refresh time…over how many cycles?
- Makes high quality validation easier and less costly

My Contact Information

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