Global Standards for the Microelectronics Industry

Get it right the first time! How to test for compliance to the LPDDR4 JEDEC Specification

Barbara Aichinger
Vice President
FuturePlus Systems Corporation
Represented in China by Fullwise Technologies

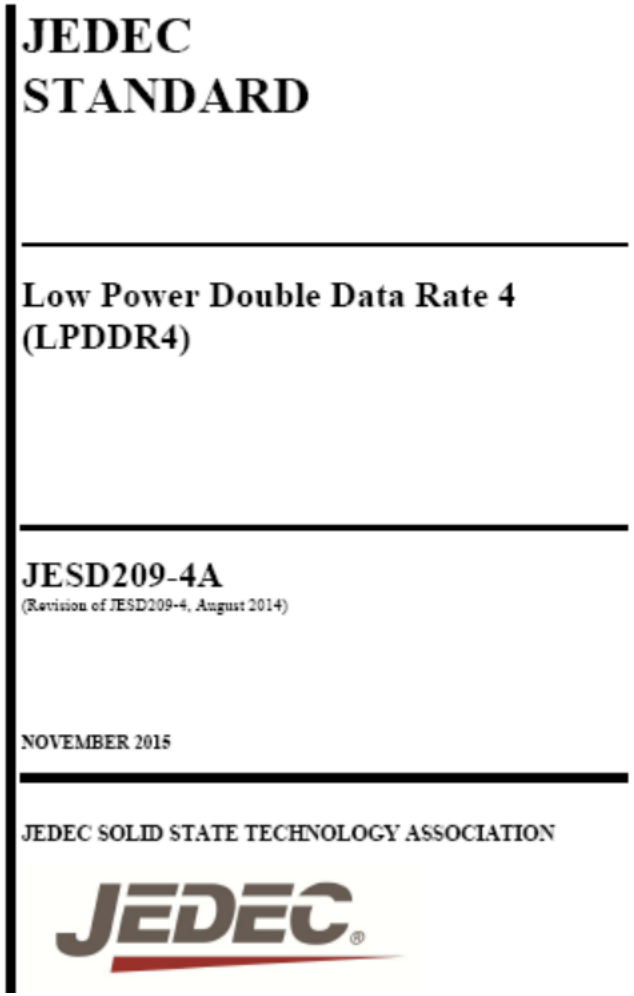
JEDEC Mobile & IOT Forum

FuturePlus Systems
Power Tools for Bus Analysis

LPDDR4 Specification

- The JEDEC LPDDR4 Specification is a *DRAM* specification
- There is no specification for the memory controller
  - Which is what you need to test!
- There is no LPDDR4 Compliance Specification

Don't Worry! Help is on the way!


JEDEC
STANDARD

Low Power Double Data Rate 4
(LPDDR4)

JESD209-4A
(Revision of JESD209-4, August 2014)

NOVEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

What to test on your LPDDR4 design?

- That the LPDDR4 DRAM is being treated properly
  - **Electrical**
    - Signal Integrity on all signals
    - Receiver Eye size
    - BER – Bit Error Rate
  - **Protocol**
    - Protocol Checks
    - Power up /power down states
    - Performance

LPDDR4 Command/Address Rx Mask

- Do you know the difference between the 'Mask' and the Data Valid Eye?

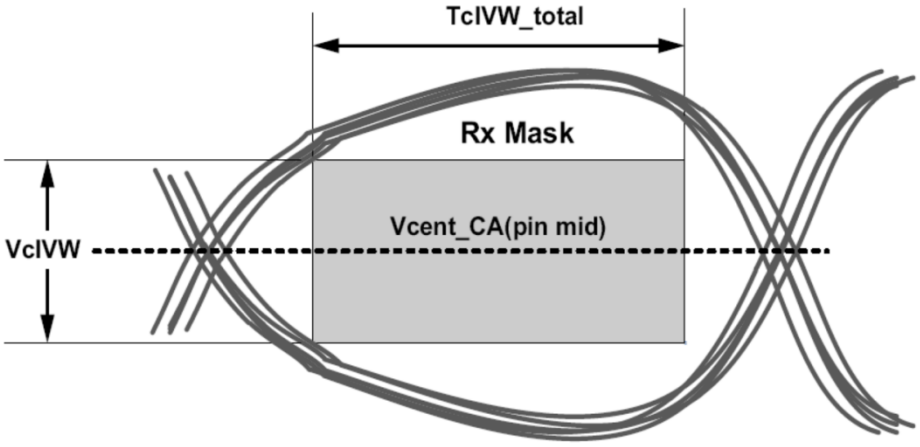


Figure 107 — CA Receiver(Rx) mask

Mask: The area (voltage and time) where no signal may encroach in order for the DRAM to successfully capture

Rx Data Valid Eye: Is the voltage/time opening measured at the receiver

DQ Data Rx Mask

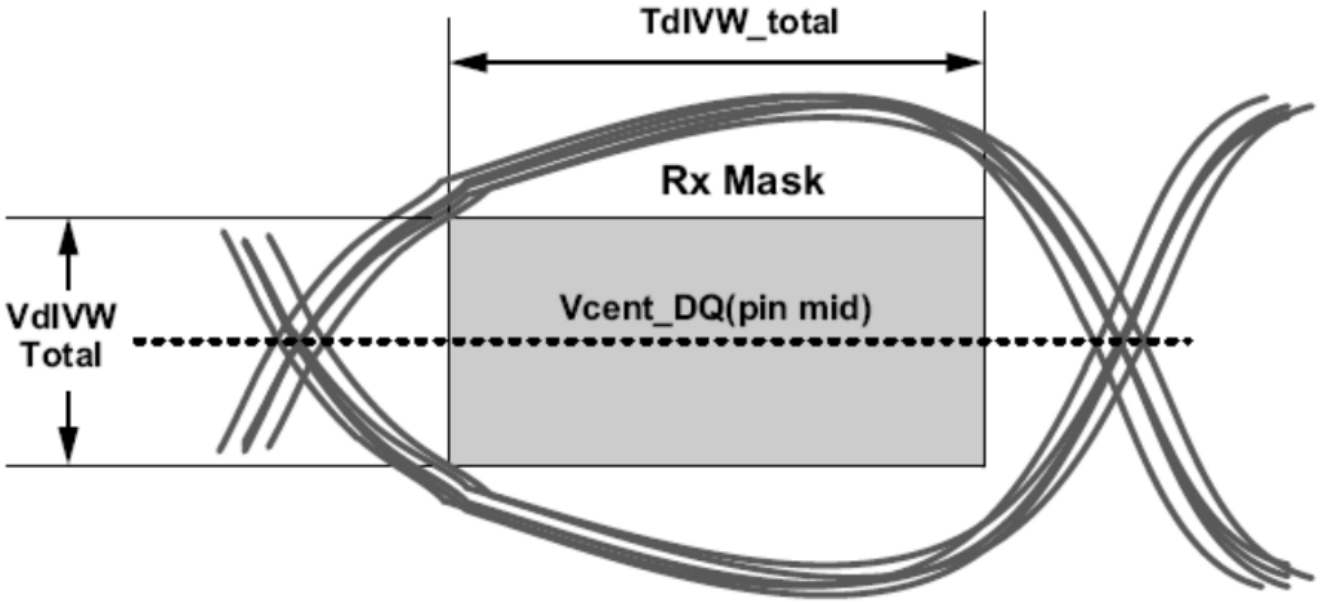
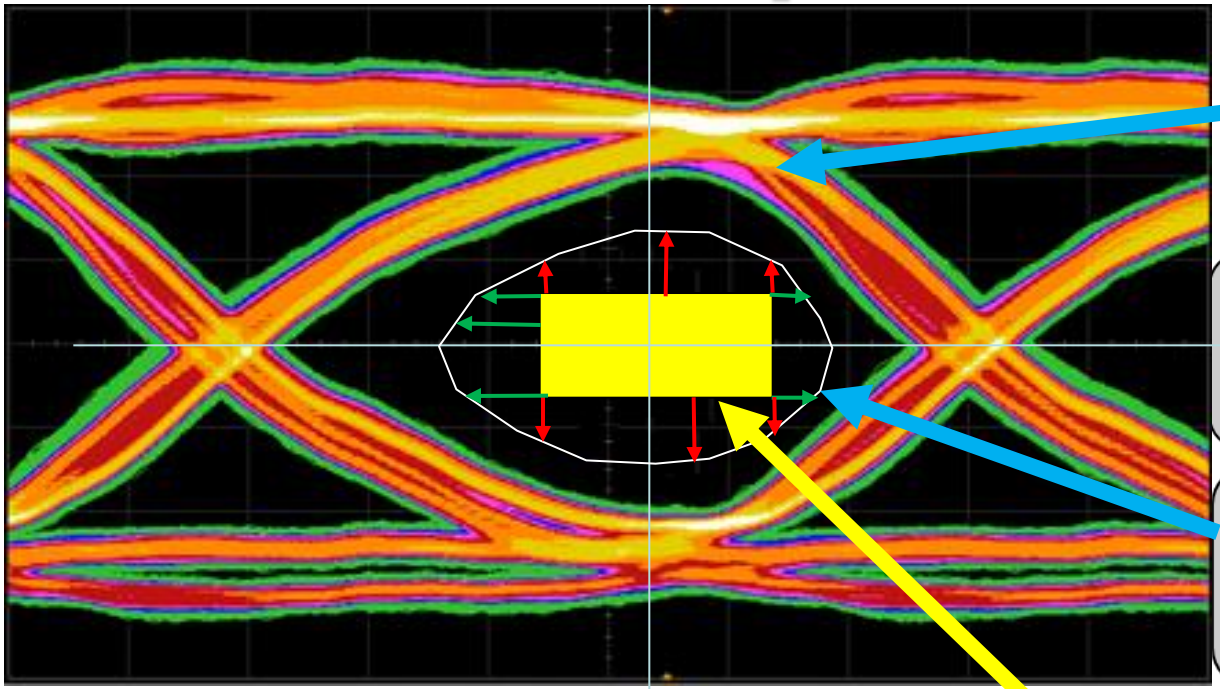


Figure 114 — DQ Receiver(Rx) mask

Measuring System Compliance



About 1E6 bits accumulated by scope at DRAM pin

Vcent (one for all DQs, one for all CAs)

Dual-dirac eye extra-polation to (TBD) BER (approx. 1E-9 to 1E-16)

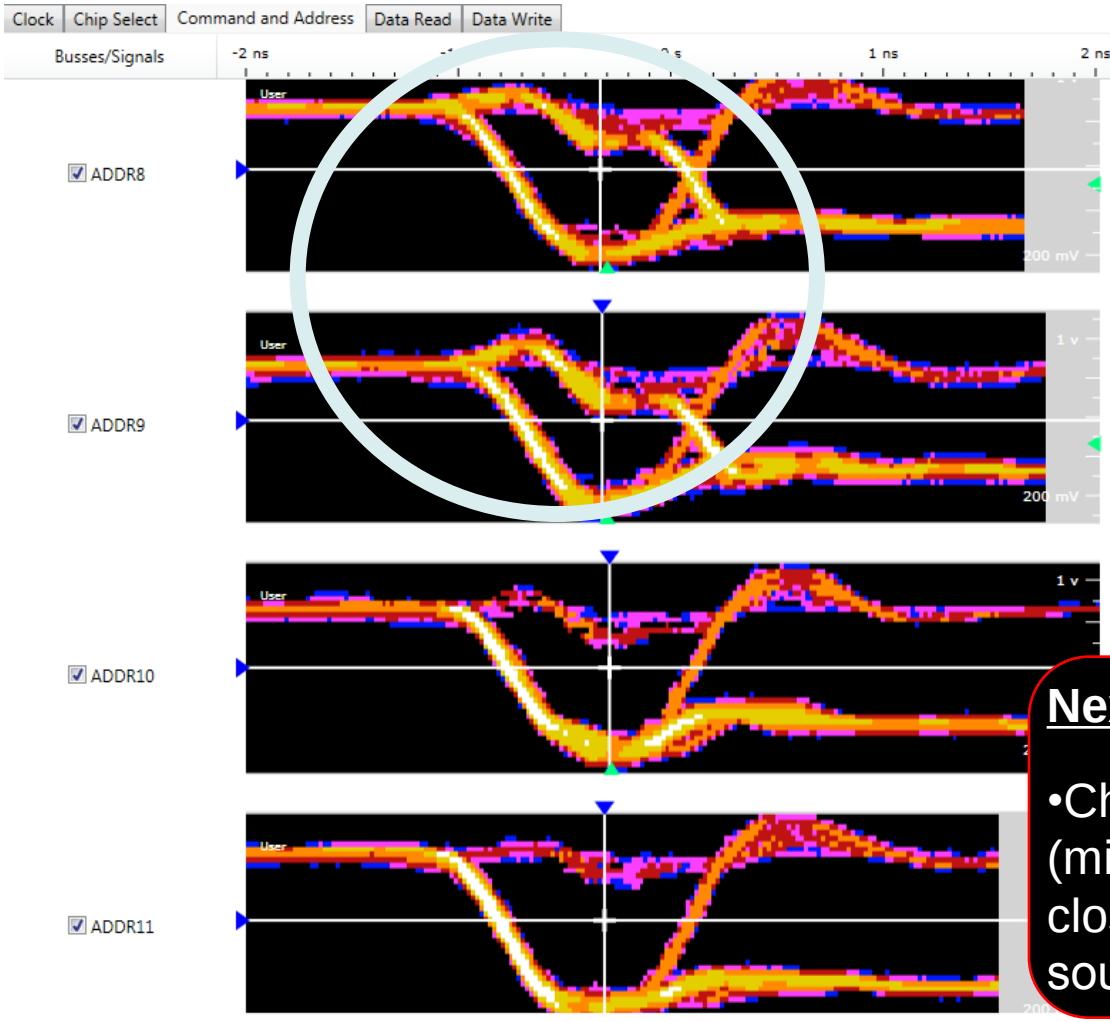
Mask center time calculated separately for each signal

Extrapolated eye must **not** touch the mask

LPDDR4 Bus Level Signal Integrity Insight

- A quick way to get bus level signal integrity insight is to use a logic analyzer
  - With high speed 'scanning' capabilities
- All signals can be observed and compared to each other
- Signals with problems can be identified quickly
  - An oscilloscope then used on the problem signals

Signal Integrity Insight: Cross Talk on ADDRESS



Symptom: Random intermittent data corruption on DDR4 system

Eye Scan Insight:

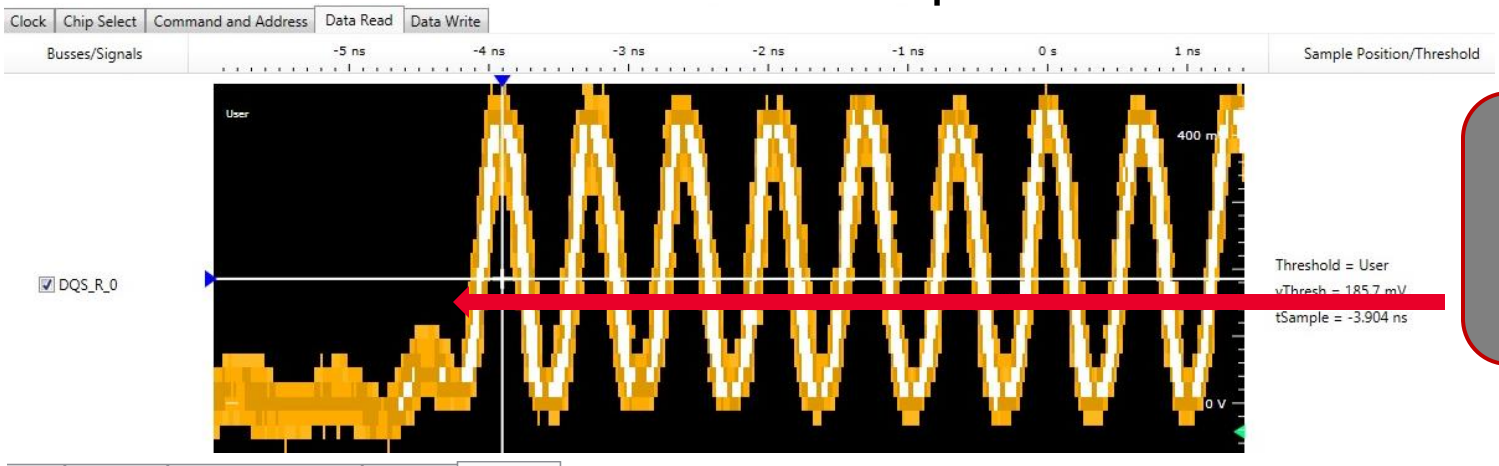
Crosstalk on ADDR 8 and ADDR9

Next Steps:

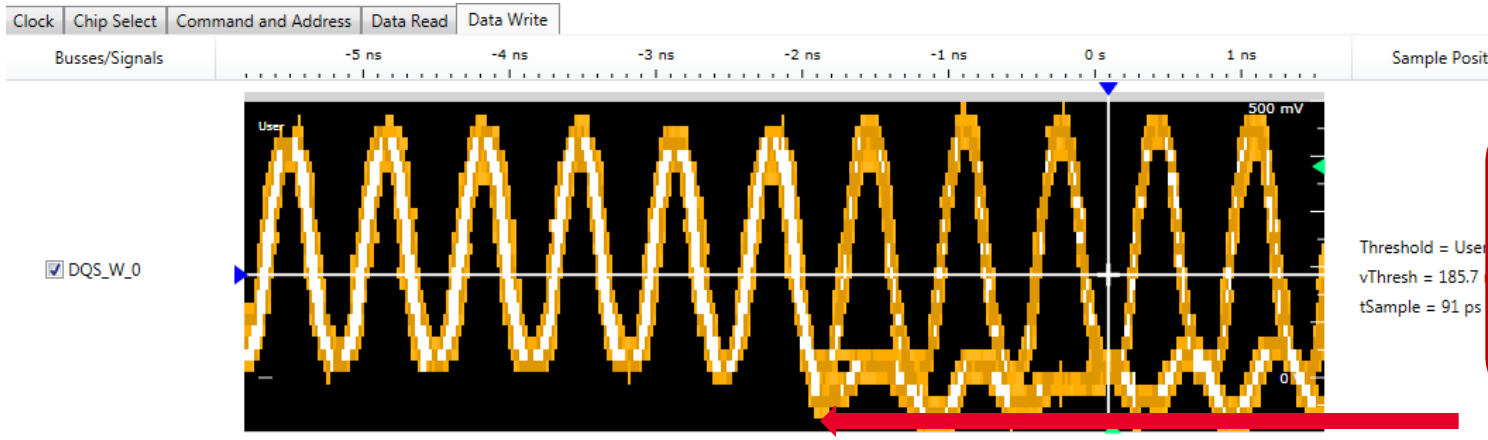
- Check routing for crosstalk threats. (missing ground planes, traces too close to each other or to noise source….)

Signal Integrity Insight: LPDDR4 DQS

Clean DQS strobes on BGA interposer for both Read/Write

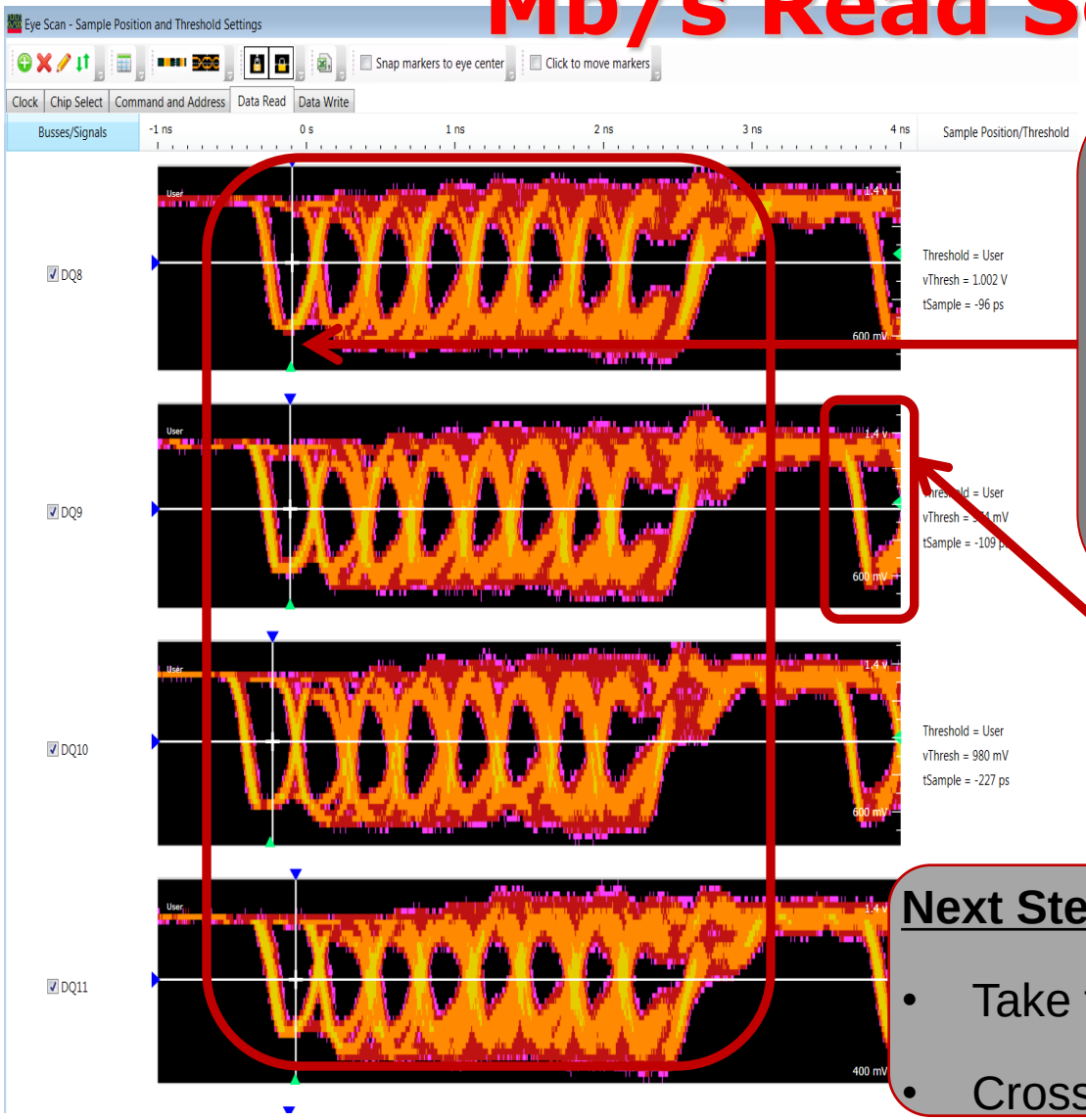


3 Gb/s Read strobe (DQS0) probed single ended.



3 Gb/s Write strobe (DQS0) probed single ended.

Signal Integrity Insight: DDR4 3500 Mb/s Read Scans



Eye Scan Insight:

- Potential ODT setting issue. Threshold of first bit in burst has less swing than remainder of burst.
- Could also be ISI (inter-symbol interference)

- Overdriving DDR4 DRAM to 1.4V could cause damage.

Next Steps:

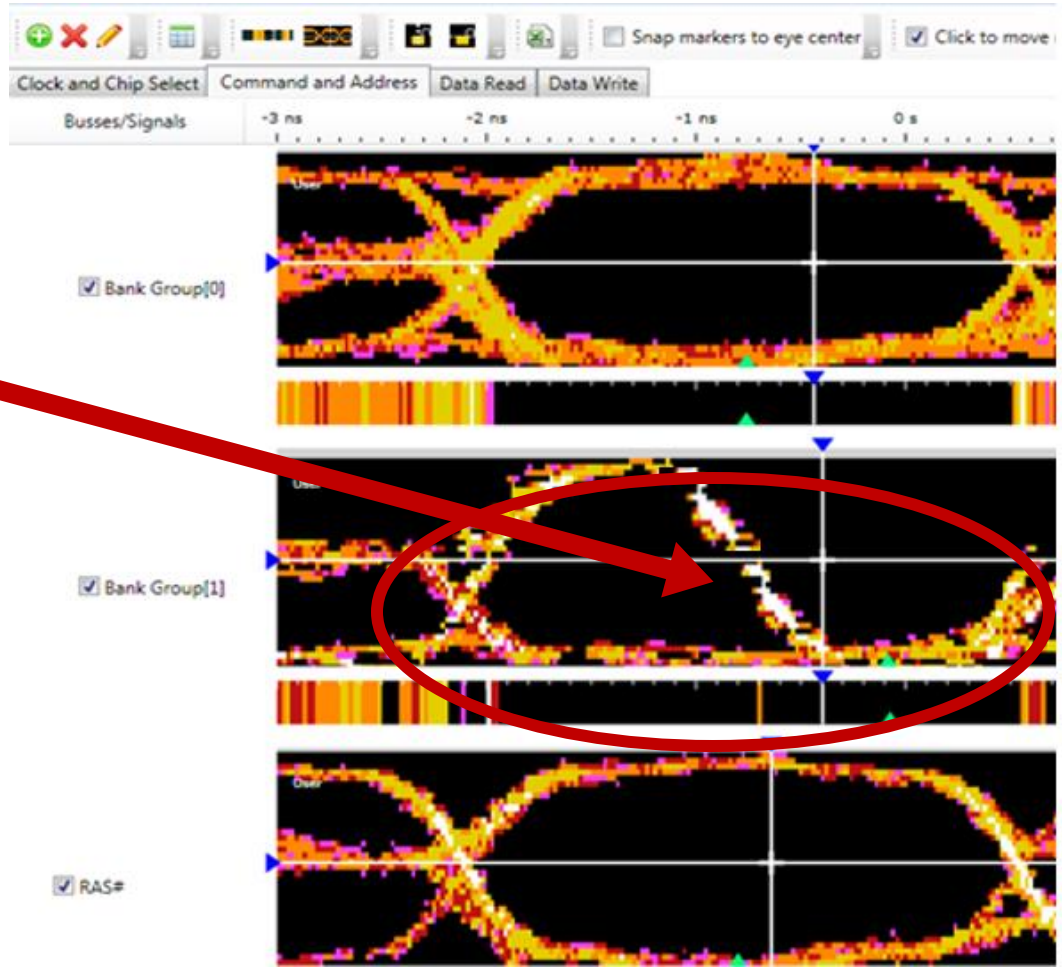
- Take trace to inspect ODT operation
- Cross trigger scope to check for ISI

Signal Integrity Insight: Incorrect Signal Transition

Symptom: Data Corruption on DDR4 system

Eye Scan Insight

DDR4 Bank Group 1 Transitioning incorrectly



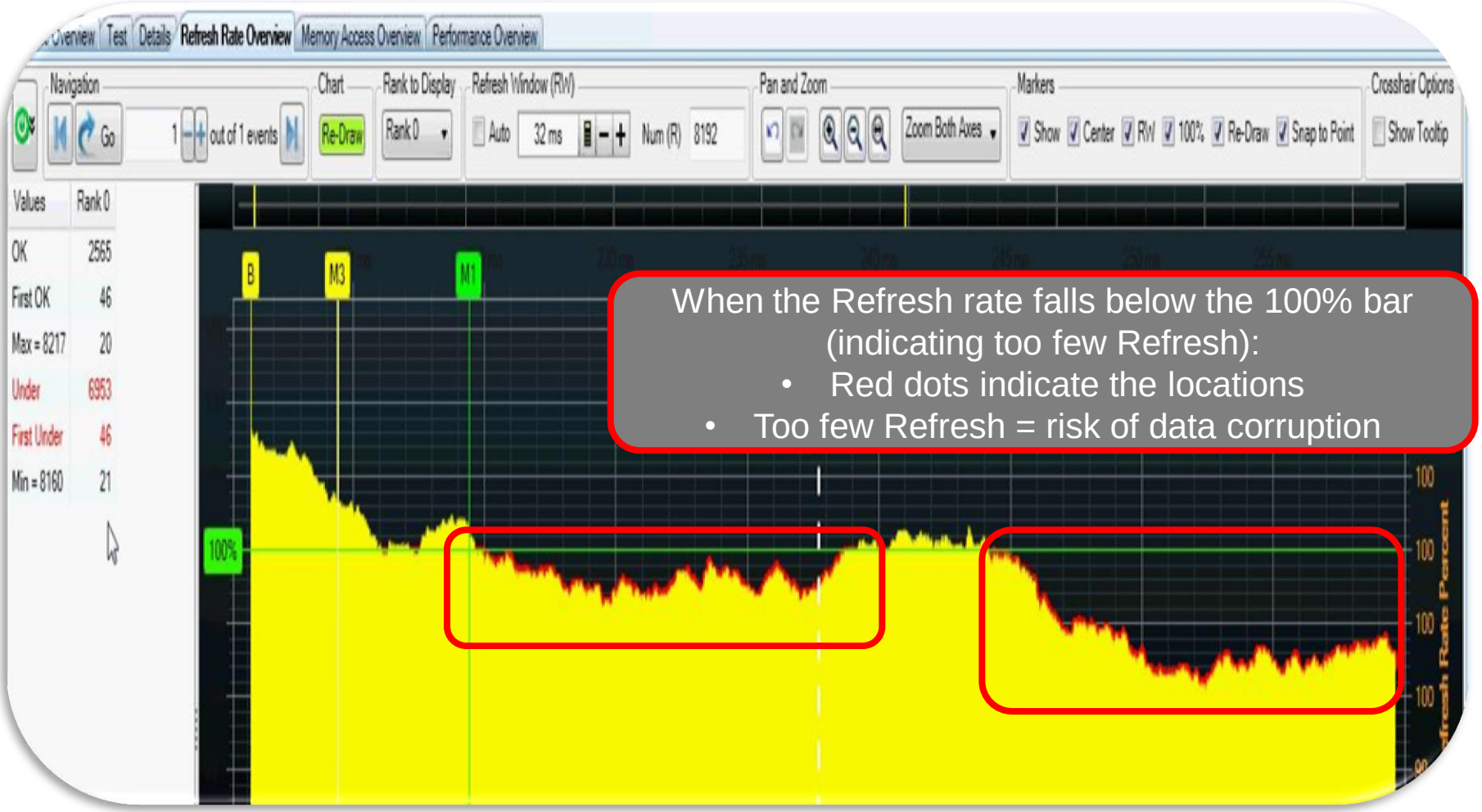
Next Steps:

- SW work around:
  - Do not use BG1 = 1
  - Limits address space
- Long term: HW fix required

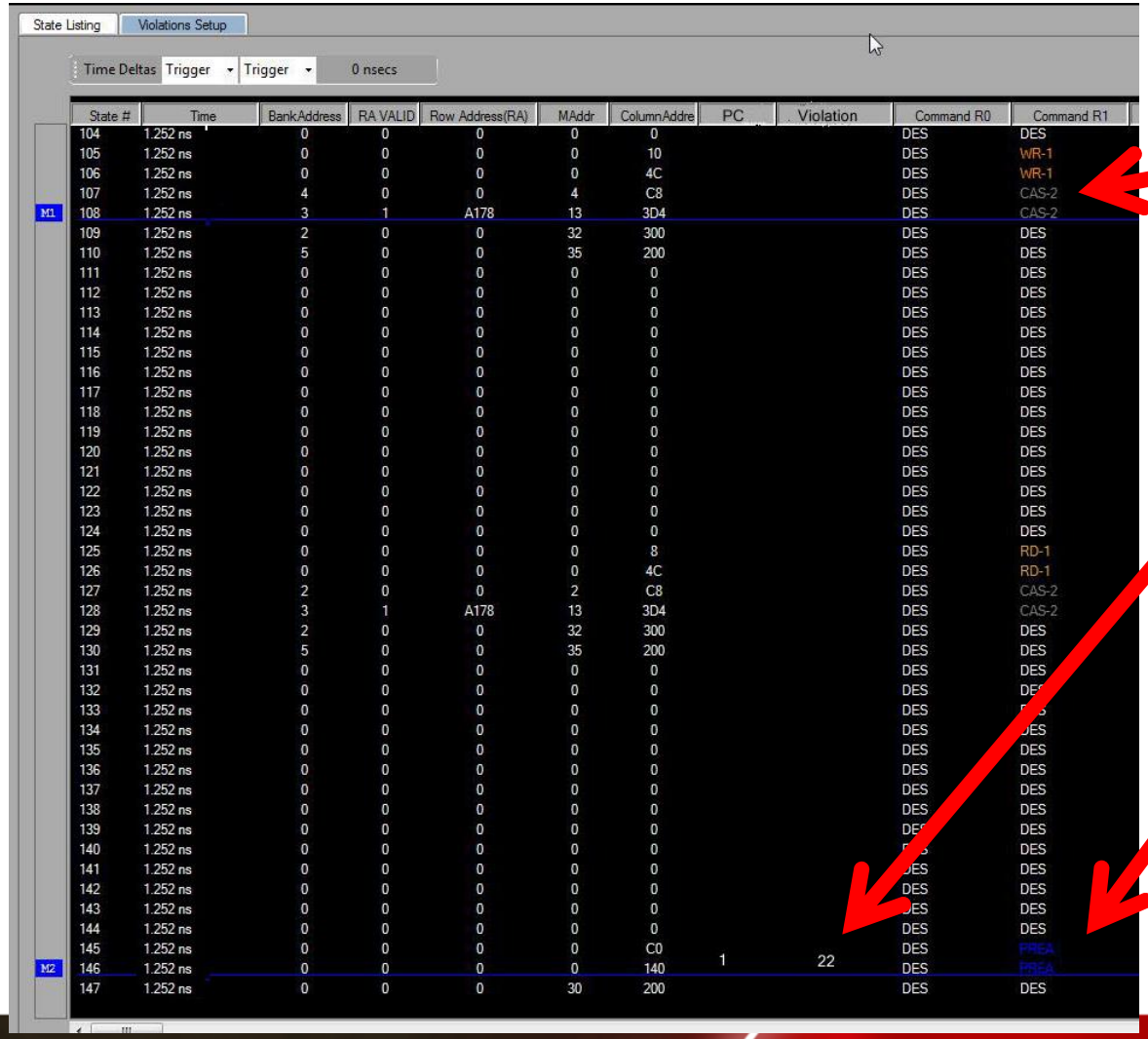
Looking for Protocol Violations

- What is a Protocol violation?
  - The specification has rules about:
    - How close in time transactions can be to each other
      - Example:Time between an ACTIVATE and a Read or Write can be no closer than tRCD
    - How far apart transactions can be from each other
      - Example:Time between two REFRESH commands cannot be greater than 9*tREFImax
    - The ordering of transactions
      - Example: A Read or Write command must be preceded with an ACTIVATE command to the selected ROW

Example: Protocol Violation Average Refresh Rate



Example: Protocol Violation
Write to close to a PREA



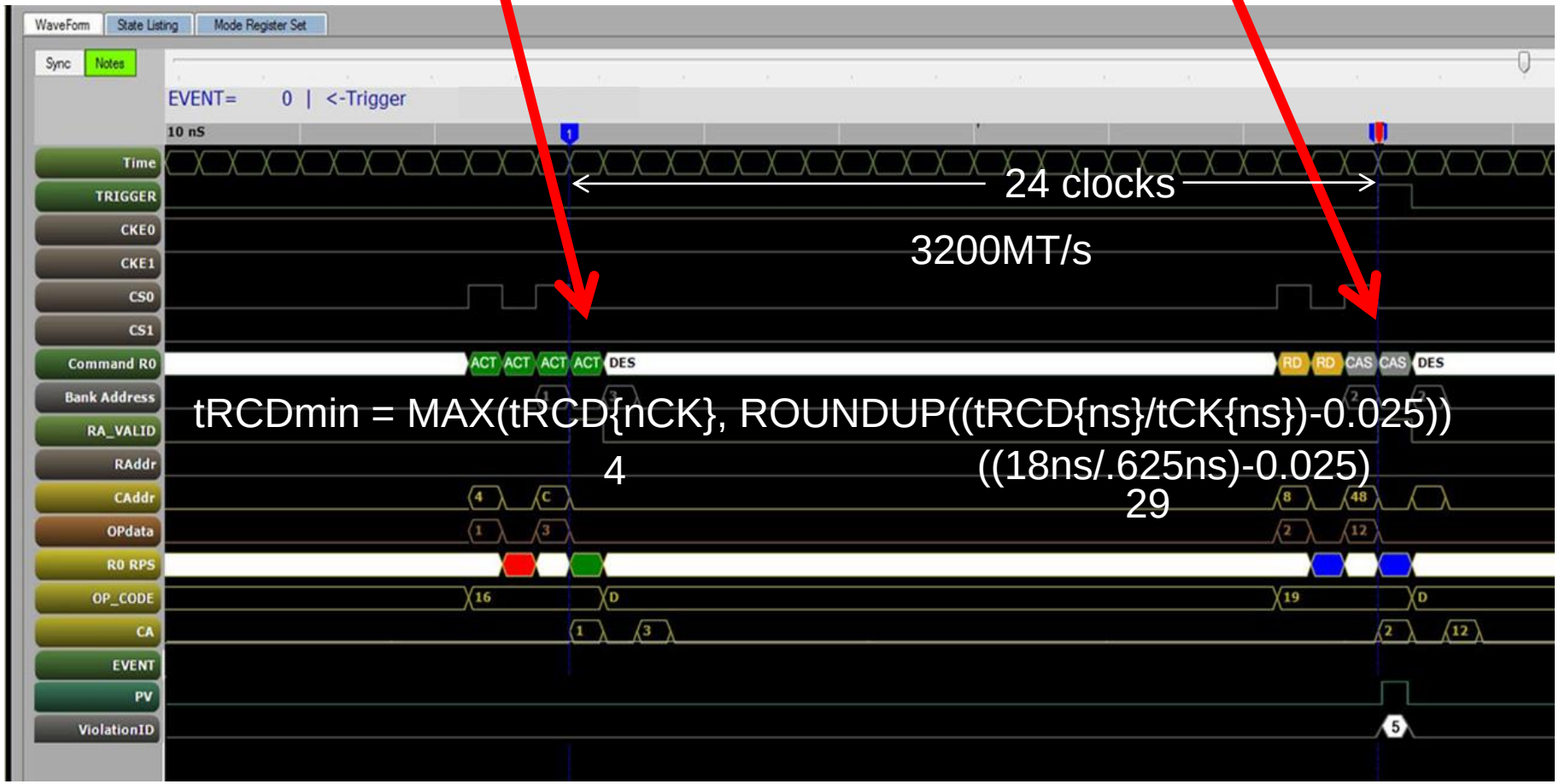
	State #	Time	BankAddress	RA VALID	Row Address(RA)	MAddr	ColumnAddre	PC	Violation	Command R0	Command R1
	104	1.252 ns	0	0	0	0	0			DES	DES
	105	1.252 ns	0	0	0	0	10			DES	WR-1
	106	1.252 ns	0	0	0	0	4C			DES	WR-1
	107	1.252 ns	4	0	0	4	C8			DES	CAS-2
M1	108	1.252 ns	3	1	A178	13	3D4			DES	CAS-2
	109	1.252 ns	2	0	0	32	300			DES	DES
	110	1.252 ns	5	0	0	35	200			DES	DES
	111	1.252 ns	0	0	0	0	0			DES	DES
	112	1.252 ns	0	0	0	0	0			DES	DES
	113	1.252 ns	0	0	0	0	0			DES	DES
	114	1.252 ns	0	0	0	0	0			DES	DES
	115	1.252 ns	0	0	0	0	0			DES	DES
	116	1.252 ns	0	0	0	0	0			DES	DES
	117	1.252 ns	0	0	0	0	0			DES	DES
	118	1.252 ns	0	0	0	0	0			DES	DES
	119	1.252 ns	0	0	0	0	0			DES	DES
	120	1.252 ns	0	0	0	0	0			DES	DES
	121	1.252 ns	0	0	0	0	0			DES	DES
	122	1.252 ns	0	0	0	0	0			DES	DES
	123	1.252 ns	0	0	0	0	0			DES	DES
	124	1.252 ns	0	0	0	0	0			DES	DES
	125	1.252 ns	0	0	0	0	8			DES	RD-1
	126	1.252 ns	0	0	0	0	4C			DES	RD-1
	127	1.252 ns	2	0	0	2	C8			DES	CAS-2
	128	1.252 ns	3	1	A178	13	3D4			DES	CAS-2
	129	1.252 ns	2	0	0	32	300			DES	DES
	130	1.252 ns	5	0	0	35	200			DES	DES
	131	1.252 ns	0	0	0	0	0			DES	DES
	132	1.252 ns	0	0	0	0	0			DES	DES
	133	1.252 ns	0	0	0	0	0			DES	DES
	134	1.252 ns	0	0	0	0	0			DES	DES
	135	1.252 ns	0	0	0	0	0			DES	DES
	136	1.252 ns	0	0	0	0	0			DES	DES
	137	1.252 ns	0	0	0	0	0			DES	DES
	138	1.252 ns	0	0	0	0	0			DES	DES
	139	1.252 ns	0	0	0	0	0			DES	DES
	140	1.252 ns	0	0	0	0	0			DES	DES
	141	1.252 ns	0	0	0	0	0			DES	DES
	142	1.252 ns	0	0	0	0	0			DES	DES
	143	1.252 ns	0	0	0	0	0			DES	DES
	144	1.252 ns	0	0	0	0	0			DES	DES
	145	1.252 ns	0	0	0	0	C0			DES	PREA
M2	146	1.252 ns	0	0	0	0	140	1	22	DES	PREA
	147	1.252 ns	0	0	0	30	200			DES	DES

Last cycle of a 4 cycle **Write** Command

Time between equals WL+BL/2+tWR+1
8 +32/2+ 15 + 1
= 40 clocks
Measurement is 38 clocks: **VIOLATION**

PREA closes the bank. If this happens too quickly then the data may not be written properly

Example: Protocol Violation tRCD ACTIVATE to close to a Read



LPDDR4 Violation Spreadsheet

Made available by FuturePlus Systems

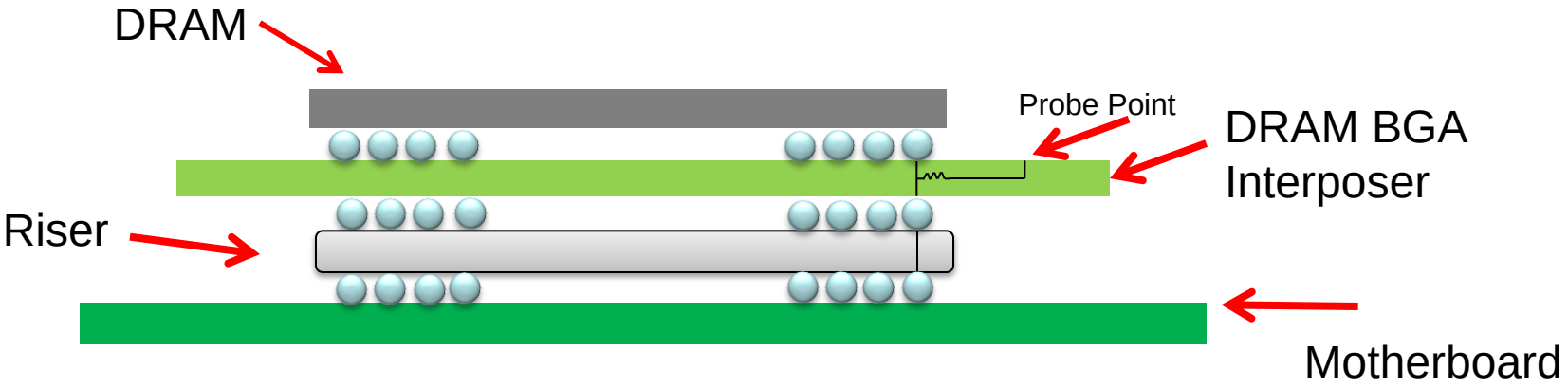
	A	B	C	D	E	F	G	H	I
4		Convert specs in time (ps) to clocks (nCK)					#CK	ns	
5		ROUNDUP((tX/tCK) -0.025) in nCKs				1600 values	A	B	1600
6			JESD209-4A		tCK	1.25 ns			1.250
7					RL	6, 10, 14, 24, 28, 32, 36			6
8				MR2 OP[5:3]	WL	4, 6, 8, 10, 12, 16, 18			4
9					tDQSCK max	3500		3500	3500
10					tRPST	0.4, 1.4			0.4
11					BL	16, 32			16
12					tWPRE	1.8	1.8		1.8
13									
14	tRFCpb	REFpb to REFab/ACT(same bank)/	tRFCpbmin = ROUNDUP((tRFCpb{ns}/tCK{ns})-0.025)	ns		4Gb		60	48
15		REFpb(same bank) < tRFCpbmin				6Gb		90	72
16						8Gb		90	72
17		Table 35, section 4.17.1				12Gb		140	112
18						16Gb		140	112
19									
20	tRFCab	REFab to REFab/ACT/REFpb <	tRFCabmin = ROUNDUP((tRFCab{ns}/tCK{ns})-0.025)	ns		4Gb		130	104
21						6Gb		180	144
22		Table 35, section 4.17.1				8Gb		180	144
23						12Gb		280	224
24						16Gb		280	224
25									
26	tRRD	REFpb to ACT < tRRDmin	tRRDmin = MAX(tRRD{nCK},	ns			4	10	8
27		REF to REF < tRRDmin							
28									
29		Table 16, Sec 4.3							
30									
31	tRRD_ACT	ACT to ACT < tRRD_ACTmin	tRRDmin = MAX(tRRD{nCK}, ROUNDUP((tRRD{ps}/tCK{ps})-0.025))	ns			4	10	8

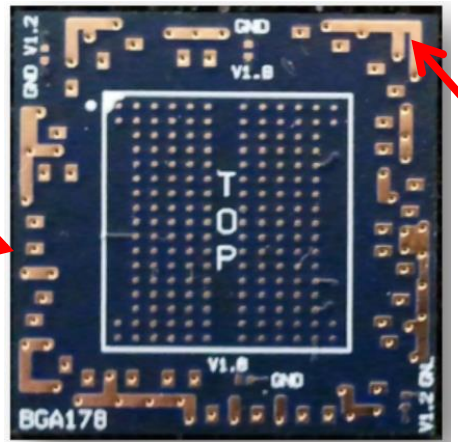
Probing

- BGA interposer
  - Flying lead
  - Midbus
  - Cable connection
- Midbus
- Slot Interposer

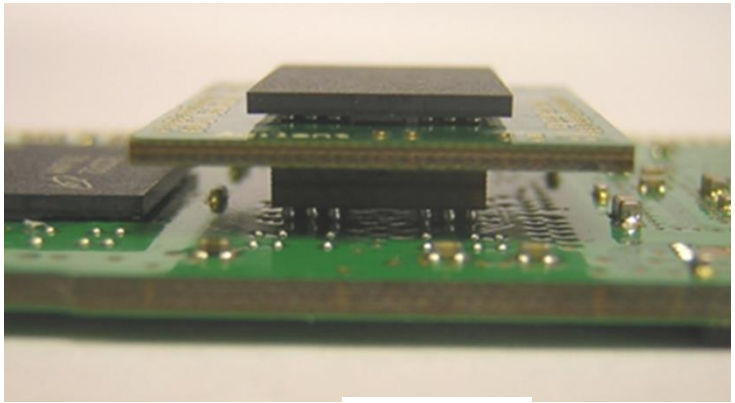
Probing LPDDR4

using a BGA interposer with individual probe points





DRAM BGA Interposer

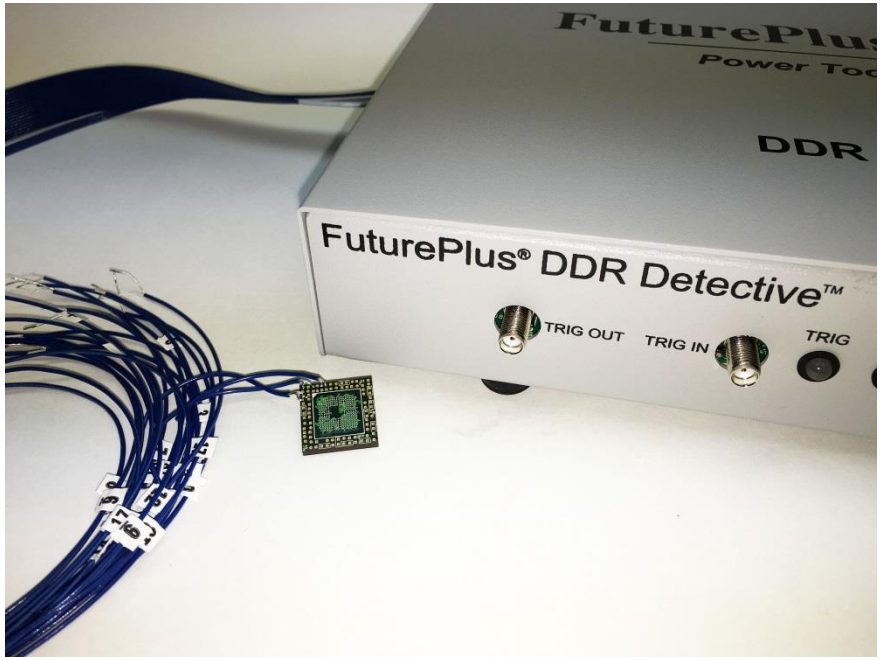


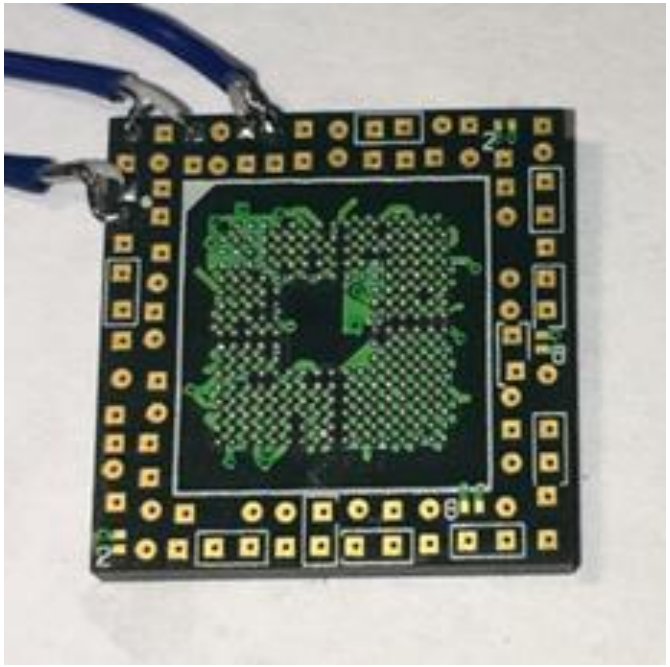
Photos Courtesy of KEYSIGHT TECHNOLOGIES

BGA probing with a scope

Photos Courtesy of KEYSIGHT TECHNOLOGIES

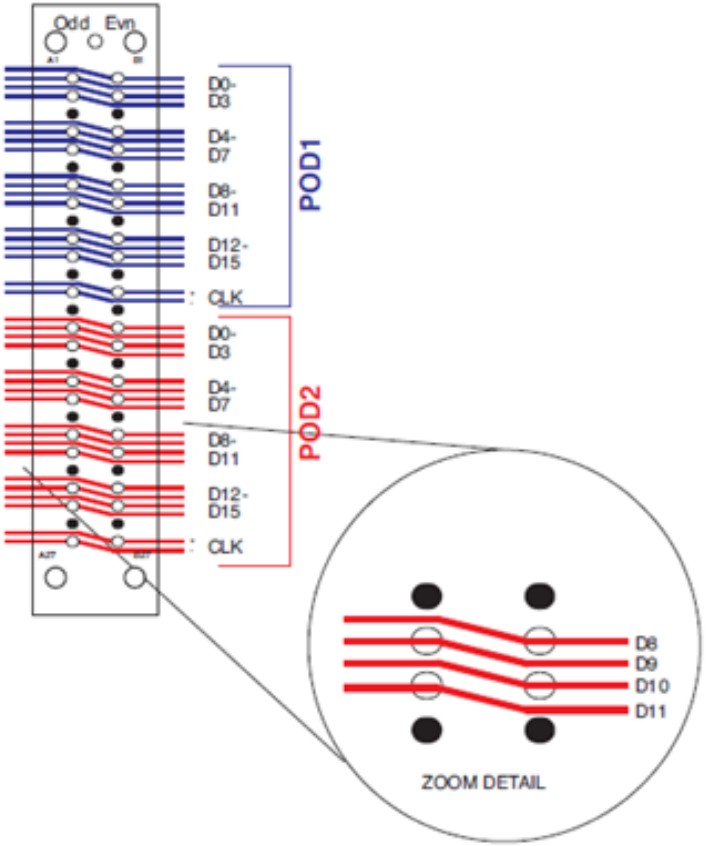
BGA Probing with a Protocol Analyzer

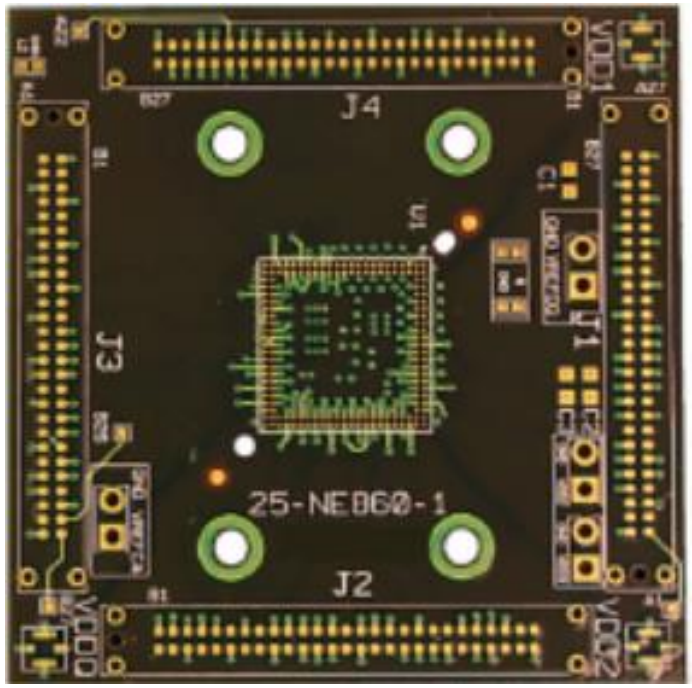




Photos courtesy of FuturePlus Systems

Midbus Footprint

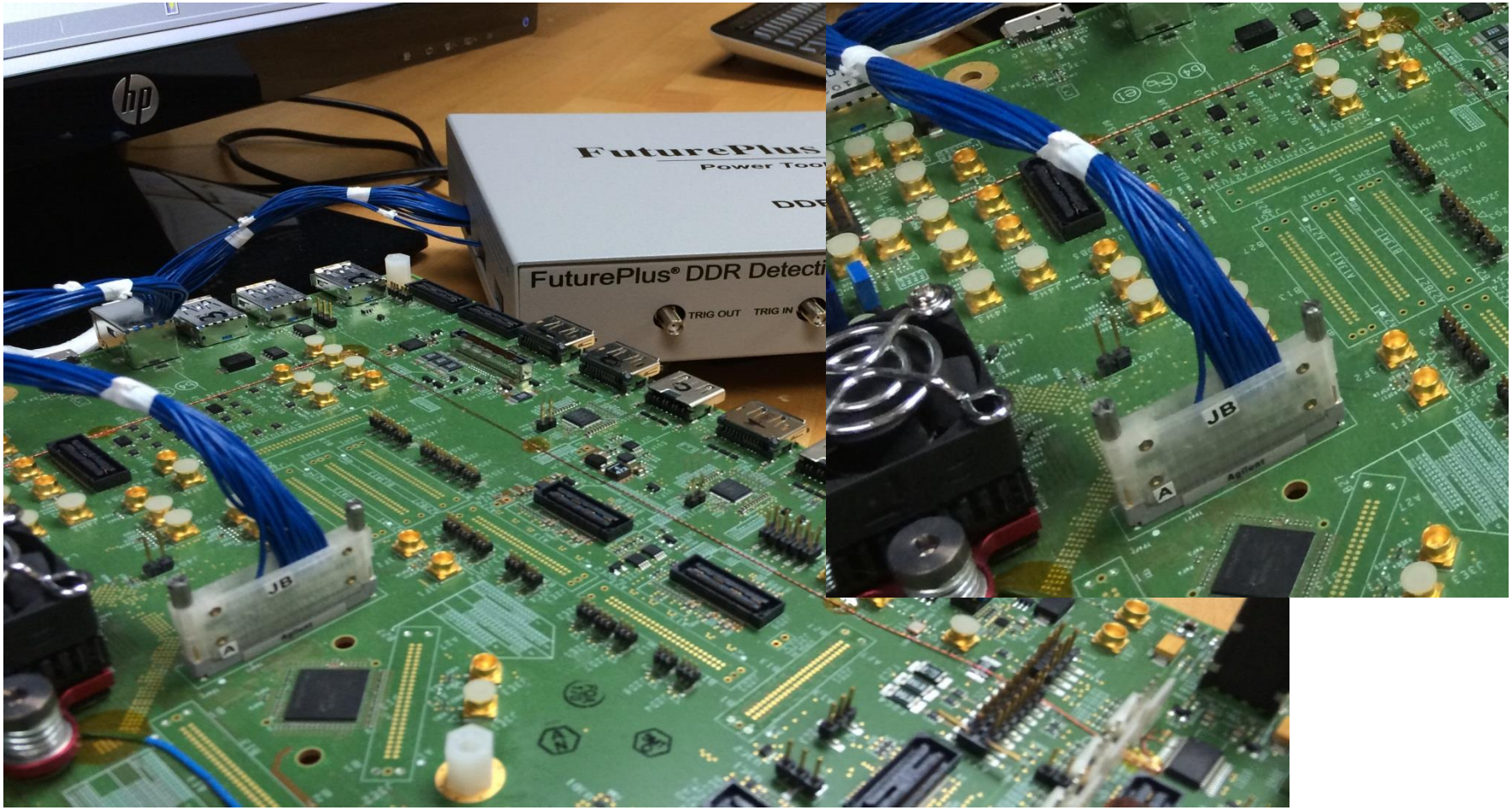




Photos Courtesy of KEYSIGHT TECHNOLOGIES

Probing LPDDR4

using a midbus footprint

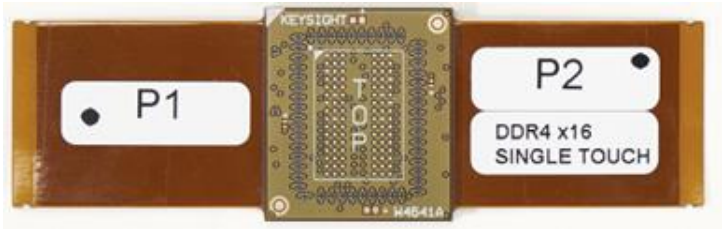


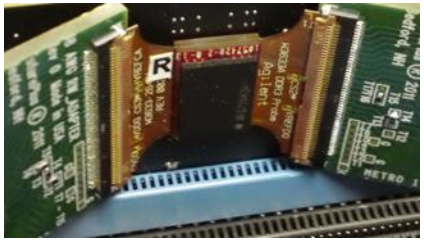
Photos courtesy of FuturePlus Systems

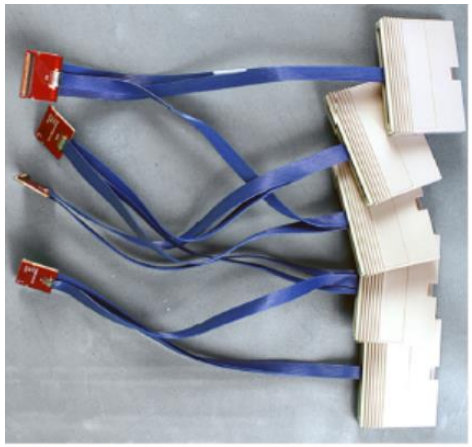
Power Tools for Bus Analysis

Probing LPDDR4

Using a BGA interposer with a cable connection to a Protocol Analyzer or Logic Analyzer

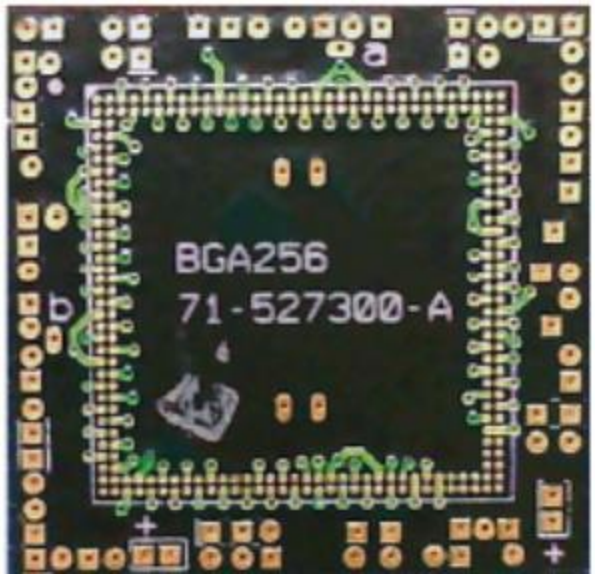






Photos Courtesy of KEYSIGHT TECHNOLOGIES

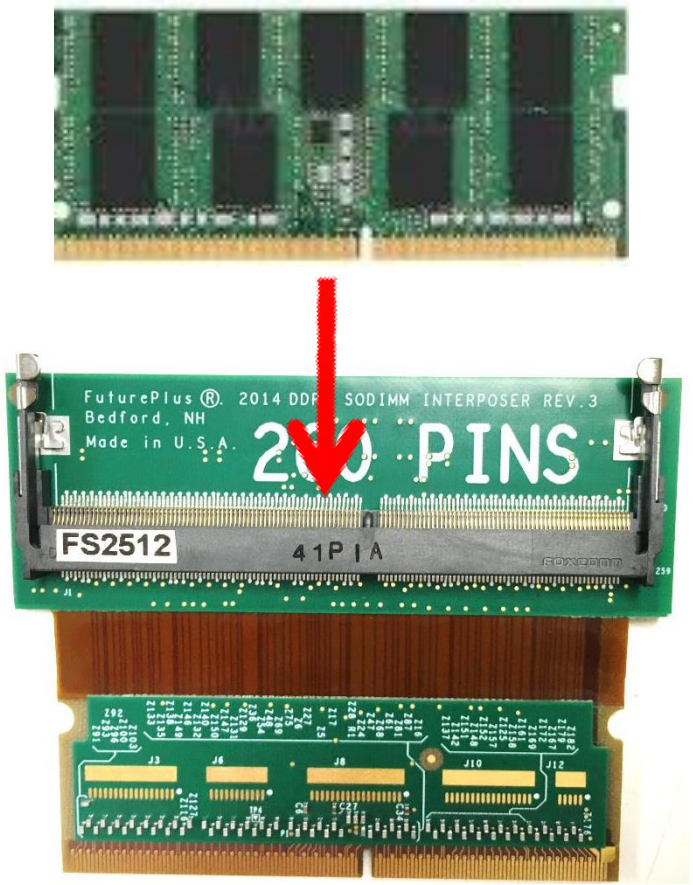
LPDDR4 Package on Package (PoP) Probing



Photos Courtesy of KEYSIGHT TECHNOLOGIES

LPDDR4 on a SODIMM

- Some applications looking at this
  - No ECC
- Will use the same form factor as DDR4 SODIMM
- Slot interposer can be used for probing



Photos courtesy of FuturePlus Systems

Equipment

Protocol Analyzer

Logic analyzer

Oscilloscope

Photos courtesy of Keysight Technologies and FuturePlus Systems

Summary for Success

- Put a robust validation and compliance plan in place for your product
- One that verifies the electrical and the protocol operation
- Plan your probing ahead of time so you can achieve success easily!

Contact Information

Barbara Aichinger
Vice President
FuturePlus Systems Corporation
15 Constitution Drive
Bedford NH 03110 USA
Barb.Aichinger@FuturePlus.com
USA 603-472-5905
www.FuturePlus.com
www.DDRDetective.com

Represented in China by Full Wise Technology
www.FullWiseTech.com